

2012 S-Series Richie 13.3" UMA/DIS Muxless Schematic

Intel Chief River Platform
Ivy Bridge (rPGA989)

Panther Point PCH

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REV:-1
2012-03-15

DY:No stuff
DIS_PX:Only DIS install

<Core Design>

緯創資通

Wistron Corporation

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Title

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(Muxless)



PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation. DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel? HD Audio dock signals to the corresponding Cougar Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. Note: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1K ohm resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2] CFG2 is for the 16x	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	1
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull down to GND through a 1KΩ ± 5% resistor to enable port	1
CFG[6:5]	PCIe Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	11
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

PCIe Routing

LANE1	X
LANE2	X
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	LAN
LANE7	X
LANE8	X

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCC3A 0D75V_S0 VCC_CORE VCC_GFXCORE VGA_CORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 ~ 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
1D5V_S3 DDR_VREF_S3	5V 1.5V	S3	
BT+ DCINOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-14.1V 9V-19.5V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

USB 2.0 Table USB3.0 Table

Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	N/A
3	N/A
4	N/A
5	N/A

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	Chief River CRV		
Device		Address	Hex	Bus
DIMM1 DIMM2 Touch-Pad				PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA
N/A				PCH_SML0_CLK/PCH_SML0_DATA
KBC G781_Thermal IC GPU_Thermal FRO G-Sensor		1001100 0X41 0X52		PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA

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CPU(1/7)

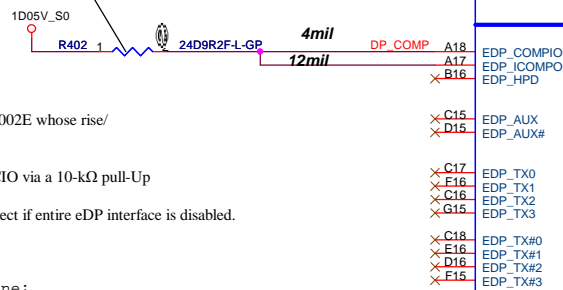
IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

DP Compensation, within 500mil



NOTE: EDP_HPDP
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns.
If HPDP on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

BOM Note: 1st/2nd/3rd Add in BOM

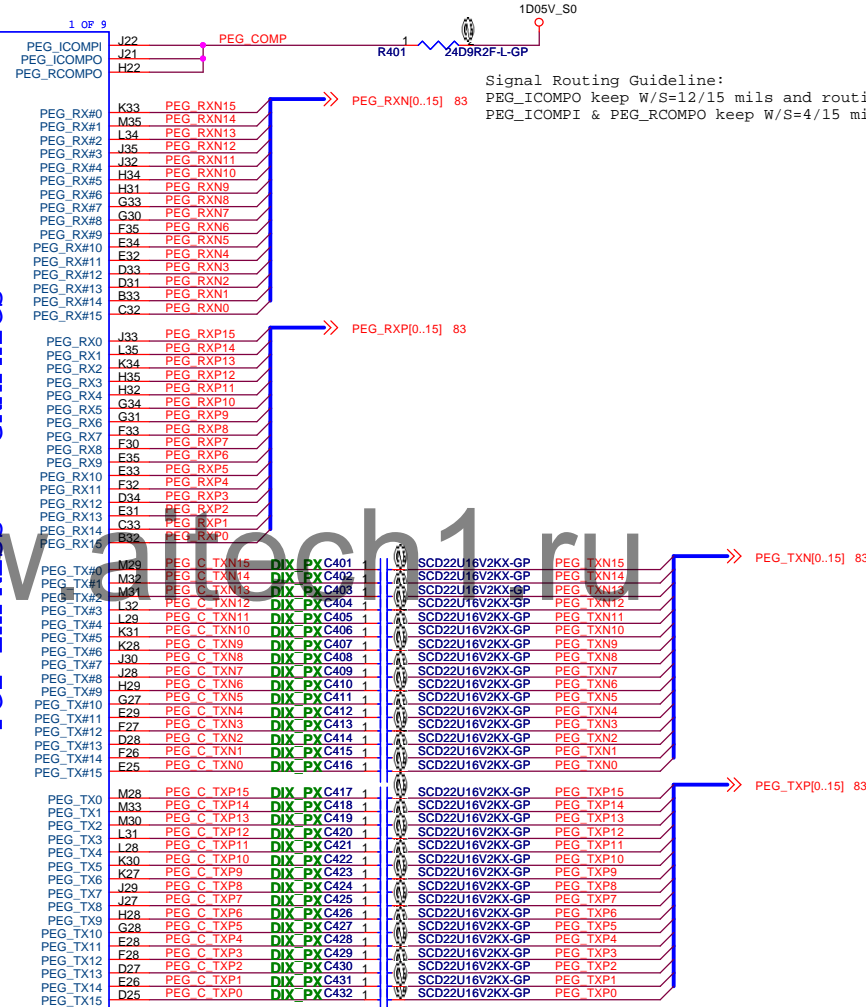
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1ST = 62.10055.551

2nd = 62.10055.321

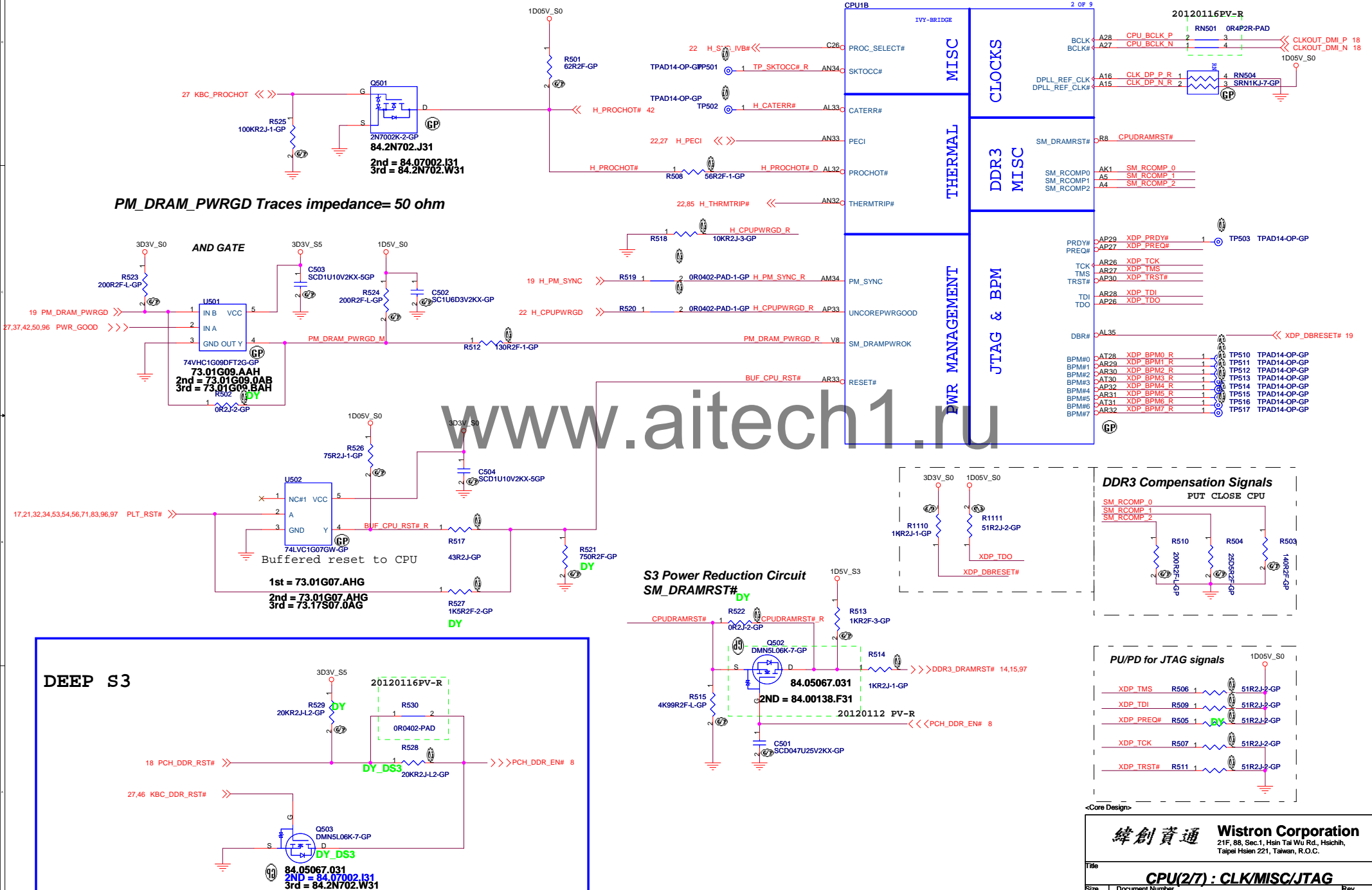
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PEG Compensation



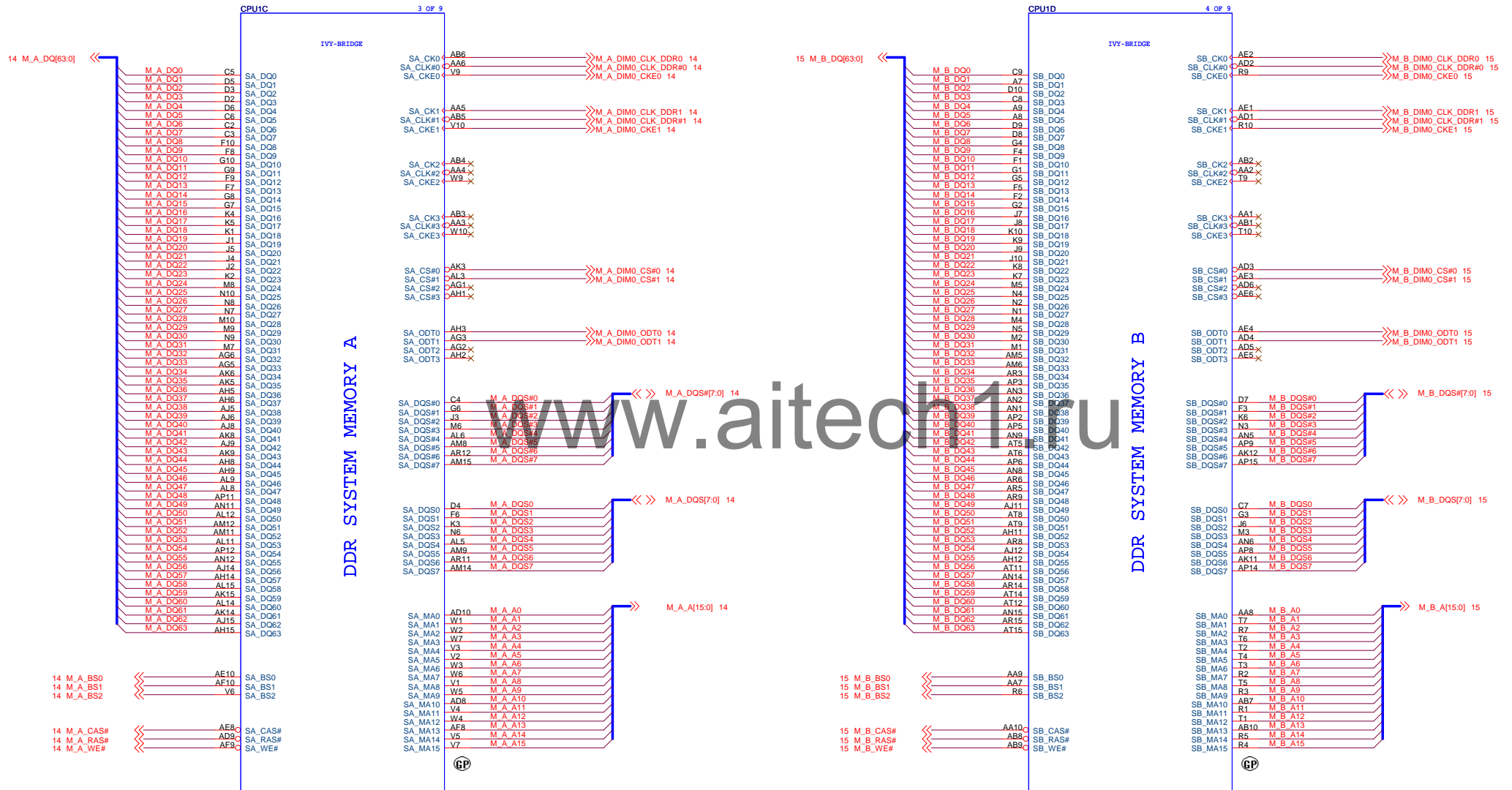
CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



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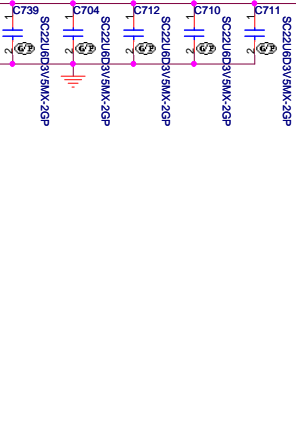
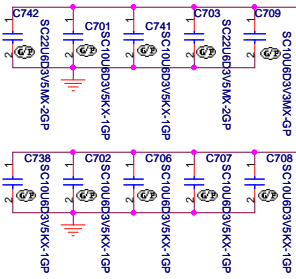
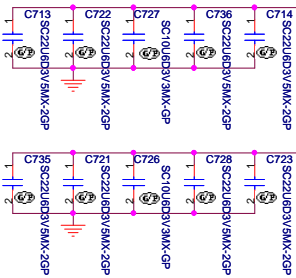
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CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

PROCESSOR CORE POWER



53A
VCC_CORE

- CPU1F
- AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AD35 VCC20
AD34 VCC21
AD33 VCC22
AD32 VCC23
AD31 VCC24
AD30 VCC25
AD29 VCC26
AD28 VCC27
AD27 VCC28
AD26 VCC29
AC35 VCC30
AC34 VCC31
AC33 VCC32
AC32 VCC33
AC31 VCC34
AC30 VCC35
AC29 VCC36
AC28 VCC37
AC27 VCC38
AC26 VCC39
AA35 VCC40
AA34 VCC41
AA33 VCC42
AA32 VCC43
AA31 VCC44
AA30 VCC45
AA29 VCC46
AA28 VCC47
AA27 VCC48
AA26 VCC49
Y35 VCC50
Y34 VCC51
Y33 VCC52
Y32 VCC53
Y31 VCC54
Y30 VCC55
Y29 VCC56
Y28 VCC57
Y27 VCC58
Y26 VCC59
Y25 VCC60
Y24 VCC61
Y23 VCC62
Y22 VCC63
Y21 VCC64
Y20 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

POWER

IVY-BRIDGE

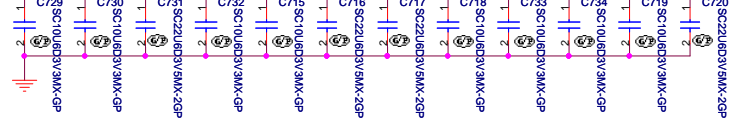
PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR UNCORE POWER



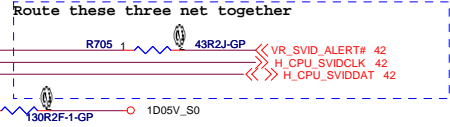
8.5A
1D05V_S0

- VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J12
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 E12
VCCIO22 E11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

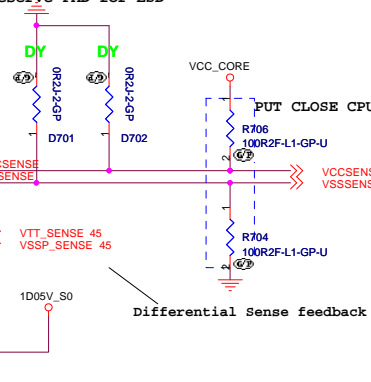
- VIDALERT#
VIDSCCLK
VIDSOUT

- VCC_SENSE
VSS_SENSE

- VCCIO_SENSE
VSS_SENSE_VCCIO



reserve PAD for ESD



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CPU(5/7)

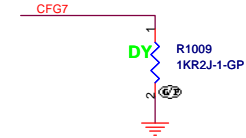
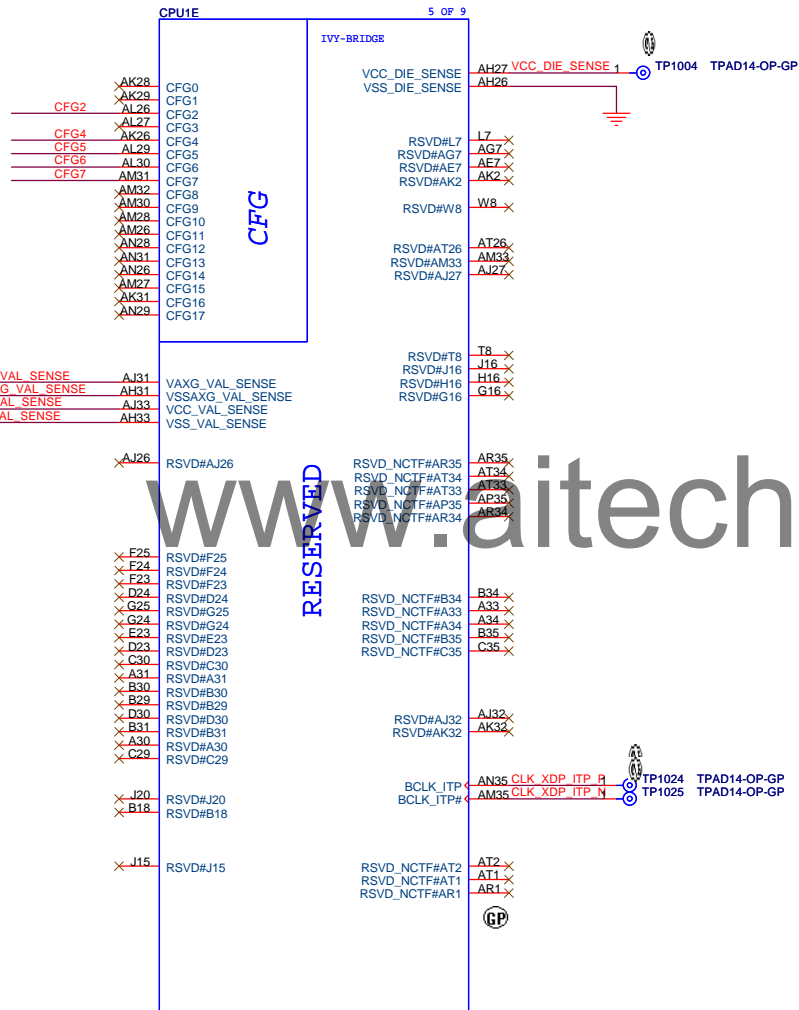


H_VCCP_SEL	Voltage
1	1.05V
0	1.0V



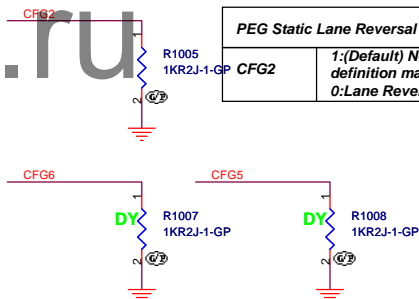
CPU(5/7) : GFX/PWR			
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IVY BRIDGE PROCESSOR (RESERVED)



Display Port Presence Strap		0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port	

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
1-GP CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

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CPU XDP

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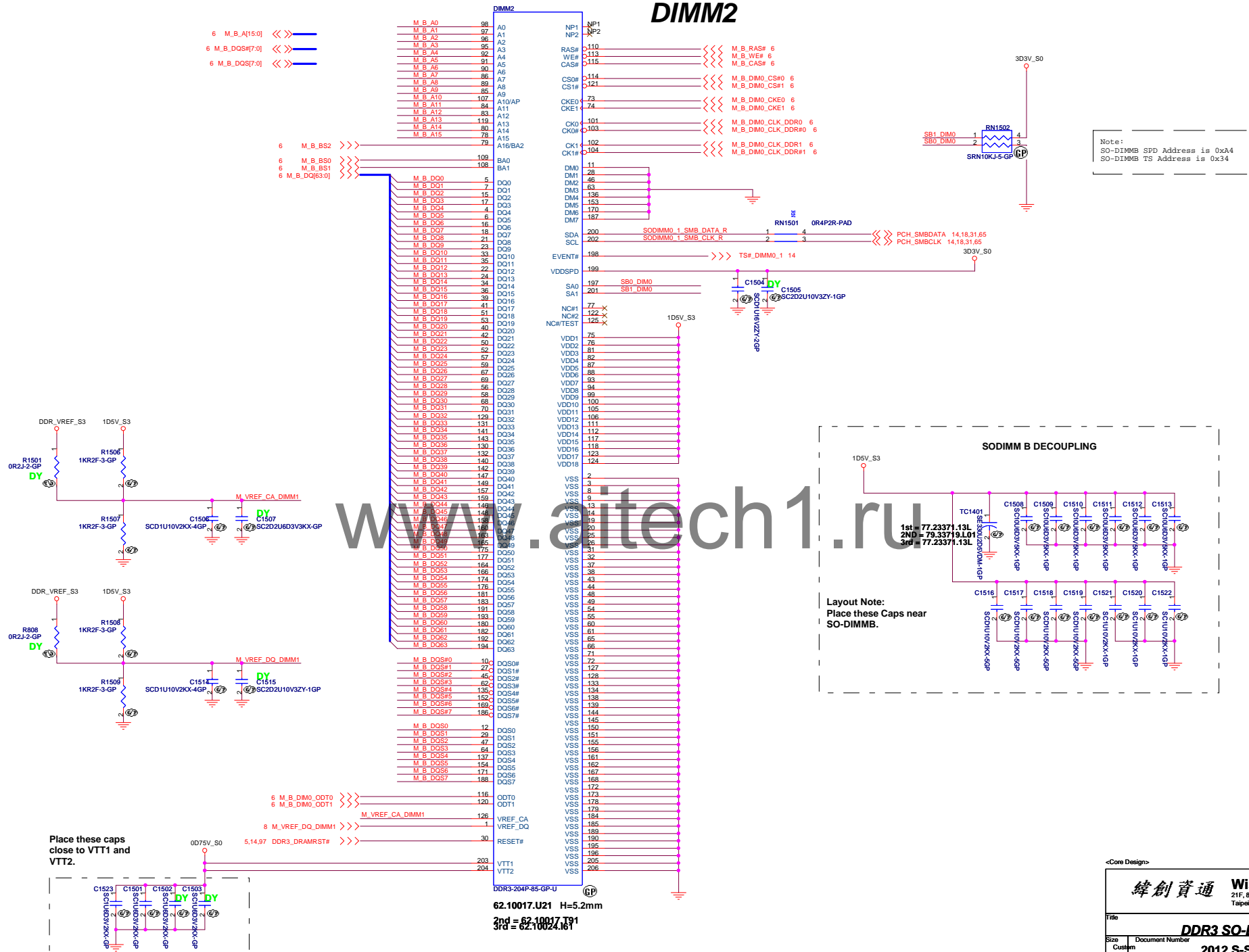
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DIMM1

M_A_DQS# [7:0] 6
 M_A_DQS [7:0] 6
 M_A_A [15:0] 6

M_A_A0	98	A0
M_A_A1	97	A1
M_A_A2	96	A2
M_A_A3	95	A3
M_A_A4	94	A4
M_A_A5	93	A5
M_A_A6	92	A6
M_A_A7	91	A7
M_A_A8	90	A8
M_A_A9	89	A9
M_A_A10	88	A10/AP
M_A_A11	87	A11
M_A_A12	86	A12
M_A_A13	85	A13
M_A_A14	84	A14
M_A_A15	83	A15
M_A_BS2	79	A16/BA2
M_A_BS0	109	BA0
M_A_BS1	108	BA1
M_A_DQ0	5	DQ0
M_A_DQ1	7	DQ1
M_A_DQ2	15	DQ2
M_A_DQ3	17	DQ3
M_A_DQ4	4	DQ4
M_A_DQ5	16	DQ5
M_A_DQ6	18	DQ6
M_A_DQ7	21	DQ7
M_A_DQ8	23	DQ8
M_A_DQ9	33	DQ9
M_A_DQ10	35	DQ10
M_A_DQ11	22	DQ11
M_A_DQ12	24	DQ12
M_A_DQ13	34	DQ13
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M_A_DQS#4	135	DQS#4
M_A_DQS#5	152	DQS#5
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M_A_DQS#7	186	DQS#7
M_A_DQS#8	193	DQS#8
M_A_DQS#9	194	DQS#9
M_A_DQS#10	195	DQS#10
M_A_DQS#11	196	DQS#11
M_A_DQS#12	197	DQS#12
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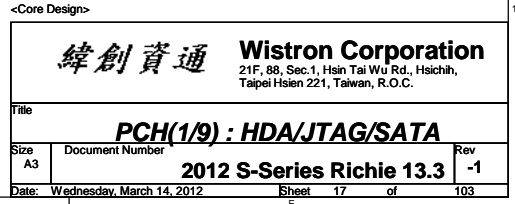
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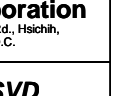
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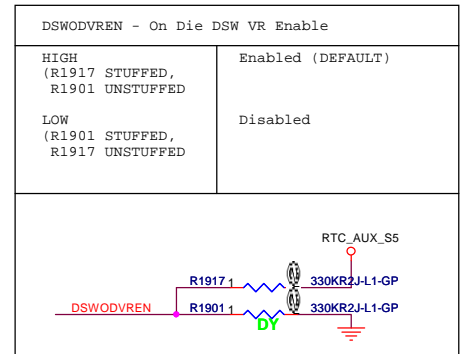
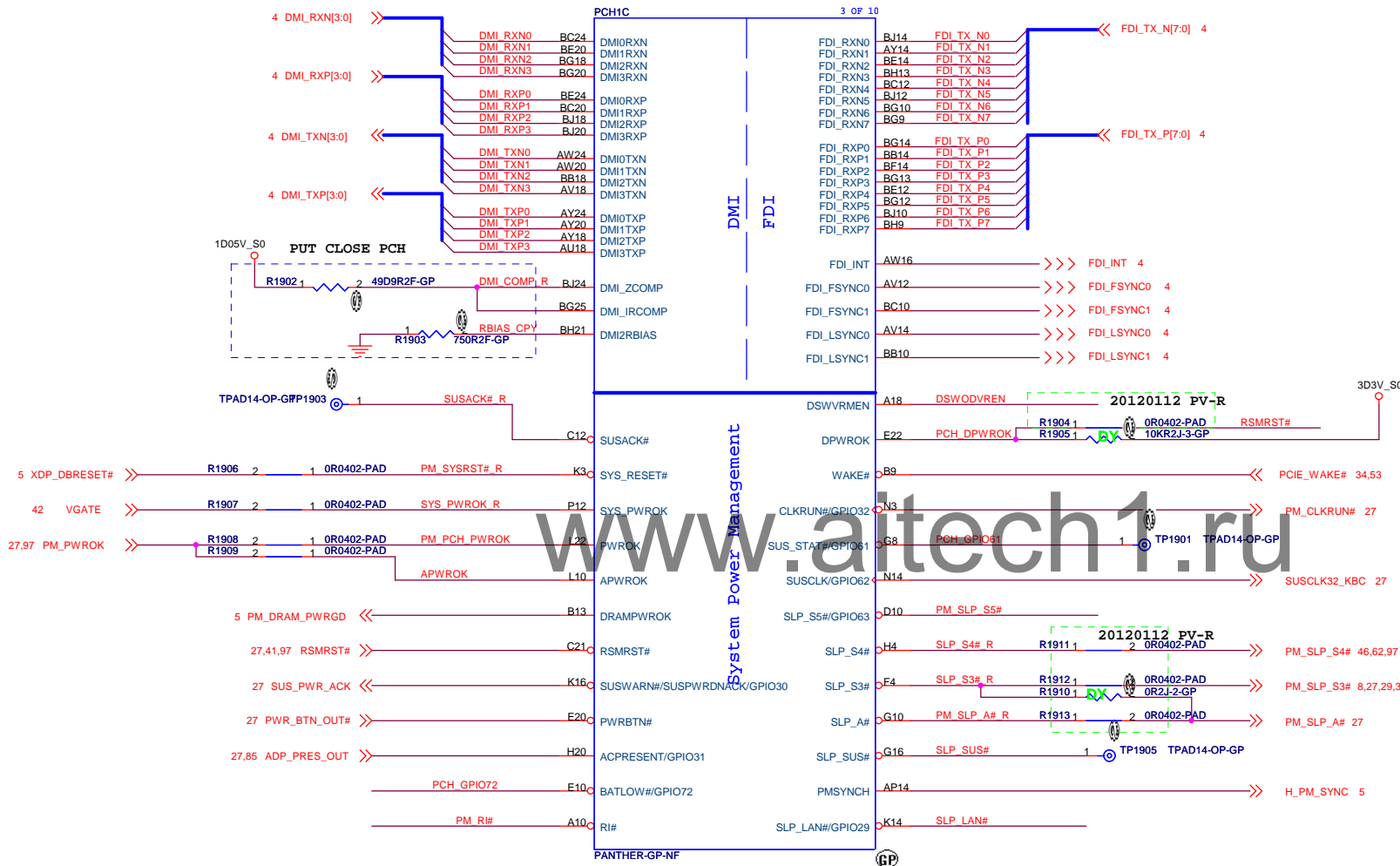
INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs



PCH1B 2 OF 10



PCH(3/9)

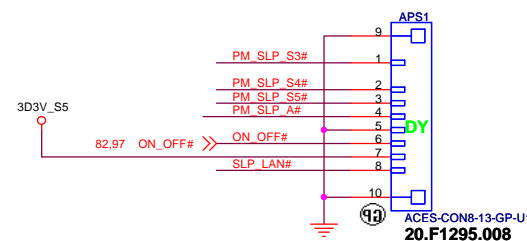


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Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC perspective.

AMT/ME COMPLIANCY TEST CONN.



<Core Design>

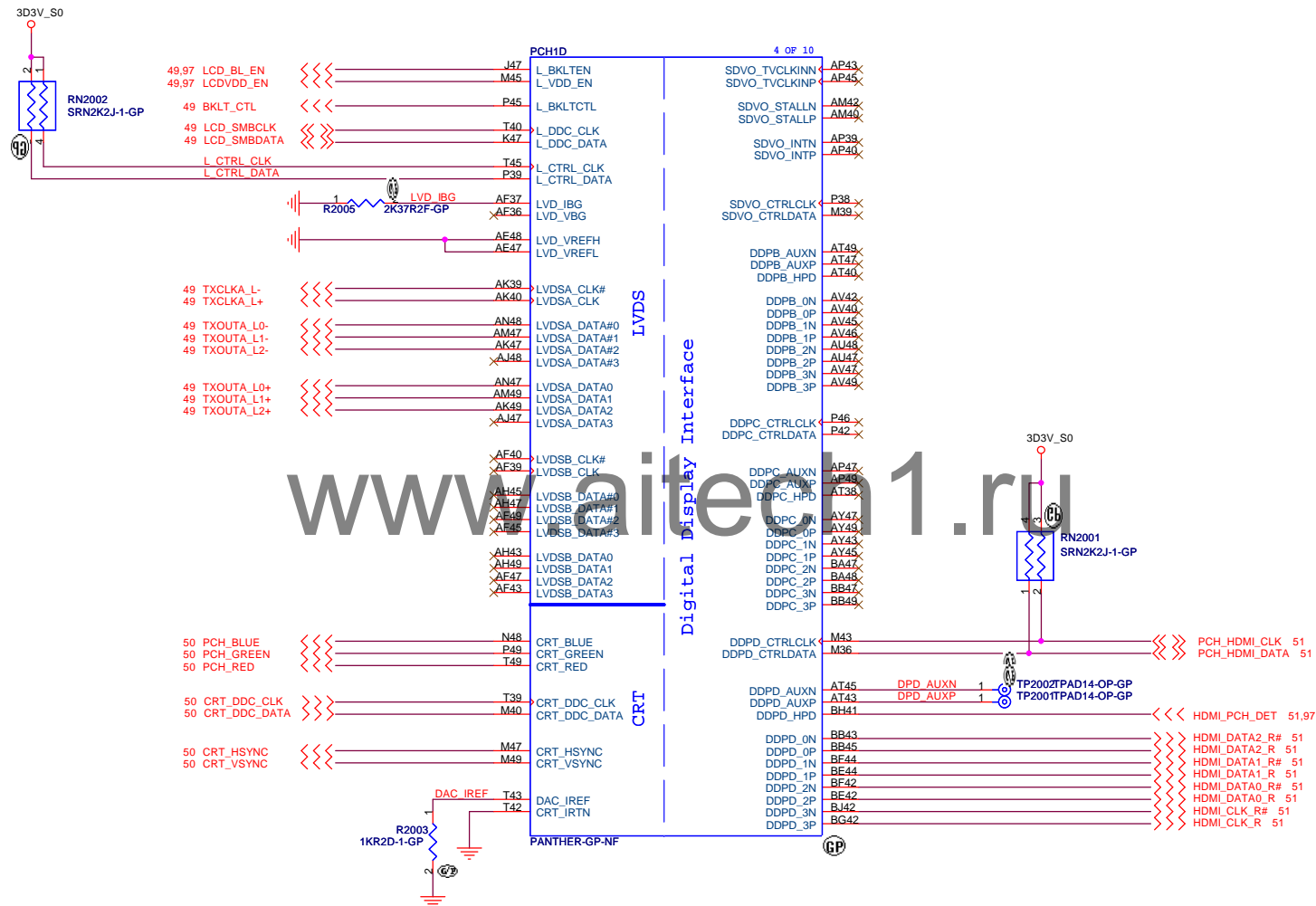
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH(3/9) : DMI/FDI/PM**

Size A3 Document Number: **2012 S-Series Richie 13.3** Rev -1

Date: Wednesday, March 14, 2012 Sheet 19 of 103

PCH(4/9)



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			PCH(4/9) : LVDS/CRT/DDI	
Size	Document Number	2012 S-Series Richie 13.3		Rev
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S 2012 Chief River	PCH GPIO 52
Richie U&D (13 inches)	1
Rocky U&D (14 inches)	1
Rocky U&D (15/17 inches)	0

S 2012 Chief River	PCH GPIO 52
Richie U&D (13 inches)	1
Rocky U&D (14 inches)	1
Rocky U&D (15/17 inches)	0

GNT1#/GPIO51	SATA1GP#/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

GNT1#/GPIO51	SATA1GP#/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

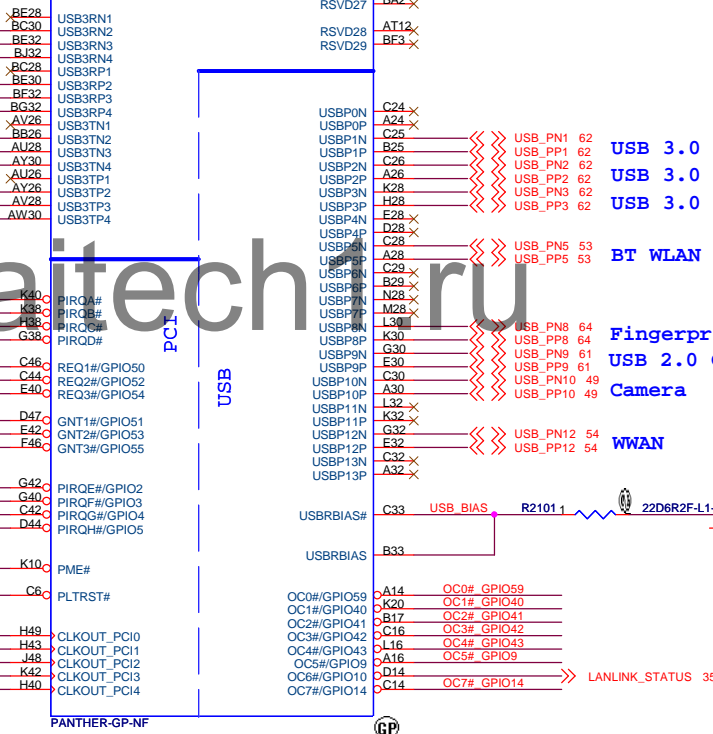
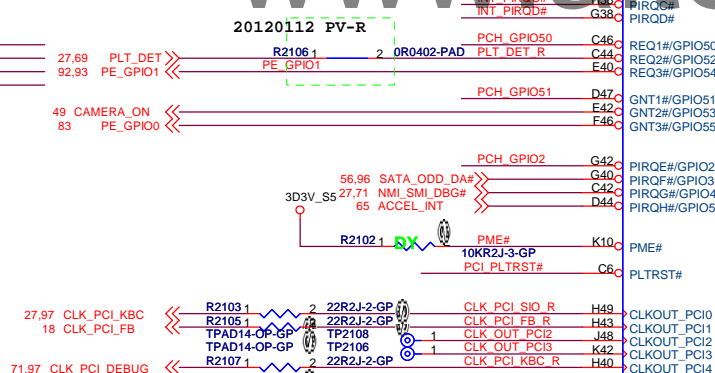
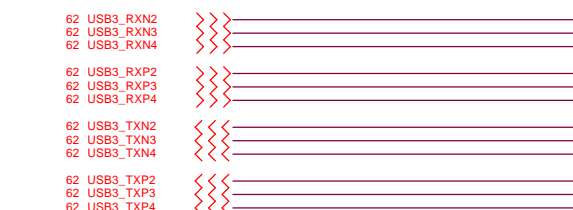
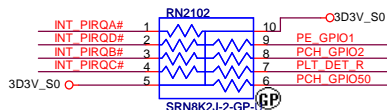
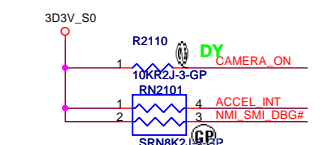
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	RSVD1 AY7
	RSVD2 AY7
TP1	RSVD3 AU3
TP2	RSVD4 BG4
TP3	
TP4	
TP5	RSVD5 AT10
TP6	RSVD6 BC8
TP7	
TP8	RSVD7 AU2
TP9	RSVD8 AT4
TP10	RSVD9 AT3
TP11	RSVD10 AY3
TP12	RSVD11 AT5
TP13	RSVD12 AV3
TP14	RSVD13 AV1
TP15	RSVD14 BB1
TP16	RSVD15 BA3
TP17	RSVD16 BB5
TP18	RSVD17 BB3
TP19	RSVD18 BB7
TP20	RSVD19 BB8
	RSVD20

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

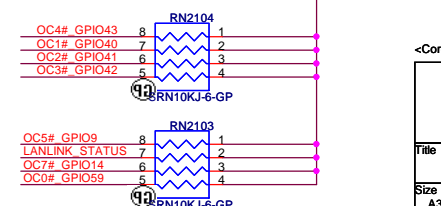
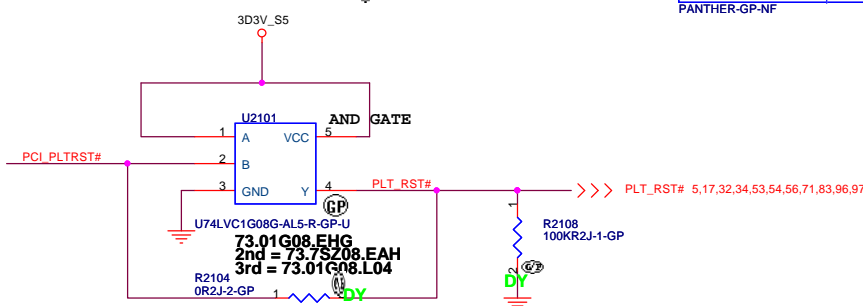
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Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3



USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

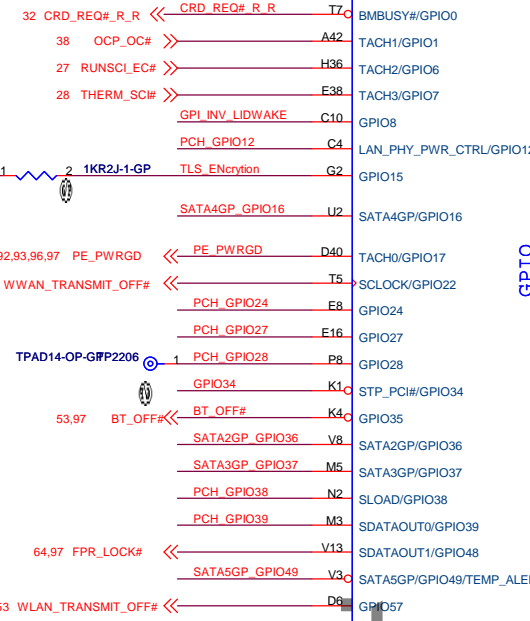
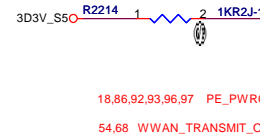
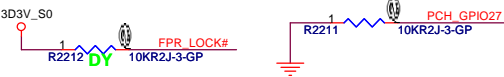
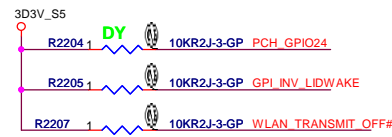
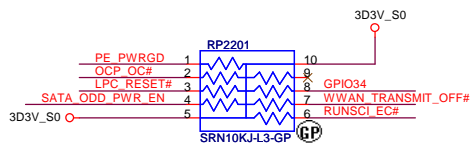
USB	
Pair	Device
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1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE



緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH(5/9) : PCI/USB/NVM			
Size	Document Number		Rev
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Date:	Wednesday, March 14, 2012	Sheet 21 of	103

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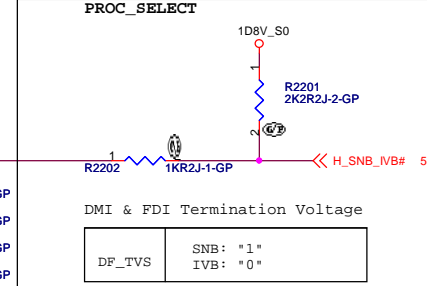
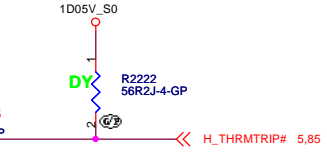
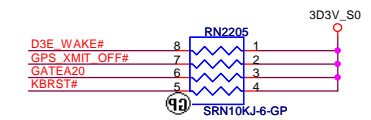


GPIO

NCIF

CPU/MISC

NCIF

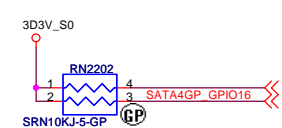
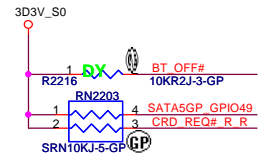
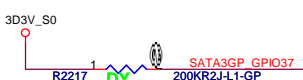
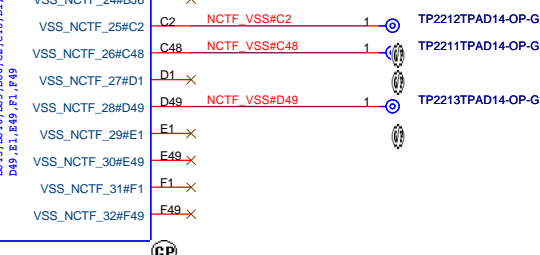
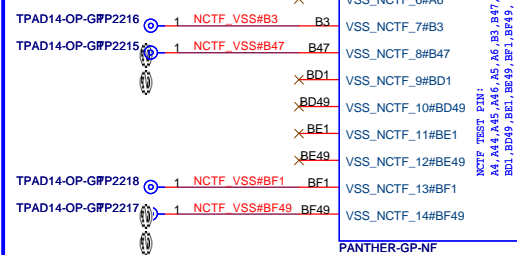


VRAM ID TABLE

PCH_GPIO39	PCH_GPIO38	VENDER
0	1	Samsung
1	0	Hynix
1	1	Elpida
0	0	UMA

GDDR5/DDR3 TABLE

20110822SI	PCH GPIO 12
Richie U&D (13 inches)	0 (13") GDDR5
Rocky U&D (14 inches)	1 (14", 15", 17") DDR3
Rocky U&D (15/17 inches)	1 (14", 15", 17") DDR3



FDI TERMINATION VOLTAGE OVERRIDE	
GPI037 (FDI_OVRVLG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPI036	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

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PCH(6/9) : GPIO/NTCF/RSVD

2012 S-Series Richie 13.3

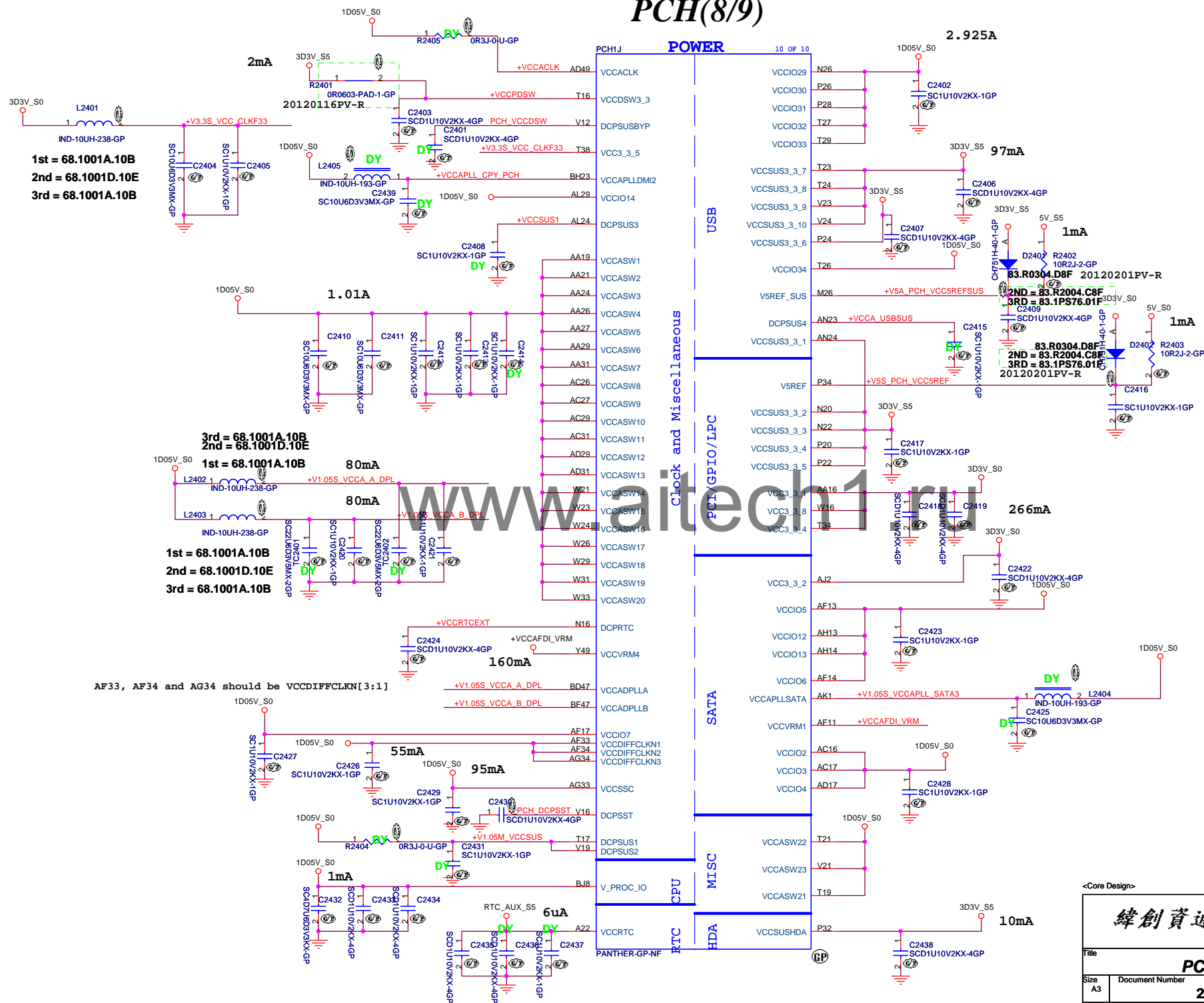
Sheet 22 of 103

PCH(7/9)



Title			
PCH(7/9) : PWR1			
Size A3	Document Number	2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012	Sheet 23	of 103	

PCH(8/9)



PCH(9/9)

PCH1I		9 OF 10
AY4	VSS159	H46
AY42	VSS160	K18
AY46	VSS161	K26
AY8	VSS162	K39
B11	VSS163	K46
B15	VSS163	K7
B19	VSS164	L18
B23	VSS165	L2
B27	VSS166	L20
B31	VSS167	L26
B35	VSS168	L28
B39	VSS169	L36
B7	VSS170	L48
F45	VSS171	M12
BB12	VSS172	M16
BB16	VSS173	M22
BB20	VSS174	M24
BB22	VSS175	M27
BB24	VSS176	M30
BB28	VSS177	M32
BB30	VSS178	M34
BB38	VSS179	M38
BB4	VSS180	M4
BB46	VSS181	M42
BC14	VSS182	M46
BC18	VSS183	M8
BC2	VSS184	N18
BC22	VSS185	P30
BC26	VSS186	N47
BC32	VSS187	P11
BC34	VSS188	P18
BC36	VSS189	T33
BC40	VSS190	P40
BC42	VSS191	P43
BC48	VSS192	VSS227
BD46	VSS193	P47
BD5	VSS194	P7
BE22	VSS195	R2
BE26	VSS196	R48
BE40	VSS197	T12
BF10	VSS198	T31
BF12	VSS199	T37
BF16	VSS200	T4
BF20	VSS201	W34
BF22	VSS202	T46
BF24	VSS203	T47
BF26	VSS204	T8
BF28	VSS205	V11
BD3	VSS206	V17
BF30	VSS207	V26
BF38	VSS208	V27
BF40	VSS209	V29
BF8	VSS210	V31
BG17	VSS211	V36
BG21	VSS212	V39
BG33	VSS213	V43
BG44	VSS214	V47
BG8	VSS215	W17
BH11	VSS216	W19
BH15	VSS217	W2
BH17	VSS218	W27
BH19	VSS219	W48
H10	VSS220	Y12
BH27	VSS221	Y38
BH31	VSS222	Y4
BH33	VSS223	Y42
BH35	VSS224	Y46
BH39	VSS225	Y8
BH43	VSS226	BG29
D3	VSS227	N24
D12	VSS228	AJ3
D16	VSS229	AD47
D18	VSS230	B43
D22	VSS231	BE10
D24	VSS232	BG41
D26	VSS233	G14
D30	VSS234	H16
D32	VSS235	T36
D34	VSS236	BG22
D38	VSS237	C22
D42	VSS238	AP13
D46	VSS239	M14
D50	VSS240	AP3
D54	VSS241	AP1
D58	VSS242	BE16
D62	VSS243	BC16
D66	VSS244	BG28
D70	VSS245	BJ28
D74	VSS246	
D78	VSS247	
D82	VSS248	
D86	VSS249	
D90	VSS250	
D94	VSS251	
D98	VSS252	
E2	VSS253	
E6	VSS254	
E10	VSS255	
E14	VSS256	
E18	VSS257	
E22	VSS258	

PCH1H		8 OF 10
H5	VSS0	
AA17	VSS1	VSS80
AA2	VSS2	VSS81
AA3	VSS3	VSS82
AA33	VSS4	VSS83
AB11	VSS5	VSS84
AB14	VSS6	VSS85
AB39	VSS7	VSS86
AB4	VSS8	VSS87
AB43	VSS9	VSS88
AB5	VSS10	VSS89
AC19	VSS11	VSS90
AC2	VSS12	VSS91
AC21	VSS13	VSS92
AC24	VSS14	VSS93
AC33	VSS15	VSS94
AC34	VSS16	VSS95
AC48	VSS17	VSS96
AD10	VSS18	VSS97
AD11	VSS19	VSS98
AD12	VSS20	VSS99
AD13	VSS21	VSS100
AD19	VSS22	VSS101
AD24	VSS23	VSS102
AD26	VSS24	VSS103
AD27	VSS25	VSS104
AD33	VSS26	VSS105
AD34	VSS27	VSS106
AD36	VSS28	VSS107
AD37	VSS29	VSS108
AD38	VSS30	VSS109
AD39	VSS31	VSS110
AD40	VSS32	VSS111
AD42	VSS33	VSS112
AD43	VSS34	VSS113
AD44	VSS35	VSS114
AD45	VSS36	VSS115
AD46	VSS37	VSS116
AD47	VSS38	VSS117
AD48	VSS39	VSS118
AE2	VSS40	VSS119
AE3	VSS41	VSS120
AE4	VSS42	VSS121
AE5	VSS43	VSS122
AE6	VSS44	VSS123
AE7	VSS45	VSS124
AE8	VSS46	VSS125
AE9	VSS47	VSS126
AE10	VSS48	VSS127
AE11	VSS49	VSS128
AE12	VSS50	VSS129
AF27	VSS51	VSS130
AF29	VSS52	VSS131
AF31	VSS53	VSS132
AF38	VSS54	VSS133
AF4	VSS55	VSS134
AF42	VSS56	VSS135
AF46	VSS57	VSS136
AF5	VSS58	VSS137
AF7	VSS59	VSS138
AF8	VSS60	VSS139
AG19	VSS61	VSS140
AG2	VSS62	VSS141
AG31	VSS63	VSS142
AG48	VSS64	VSS143
AH11	VSS65	VSS144
AH3	VSS66	VSS145
AH36	VSS67	VSS146
AH39	VSS68	VSS147
AH40	VSS69	VSS148
AH42	VSS70	VSS149
AH46	VSS71	VSS150
AH7	VSS72	VSS151
AJ19	VSS73	VSS152
AJ21	VSS74	VSS153
AJ24	VSS75	VSS154
AJ33	VSS76	VSS155
AJ34	VSS77	VSS156
AK12	VSS78	VSS157
AK3	VSS79	VSS158

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Title	
PCH(9/9) : GND	
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Title

PCH XDP

Size
A3

Document Number
2012 S-Series Richie 13.3

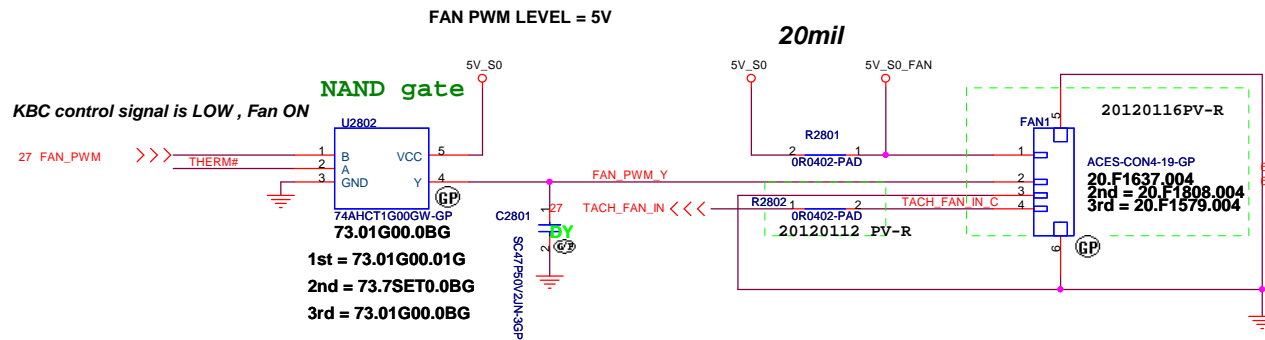
Rev
-1

Date: Wednesday, March 14, 2012

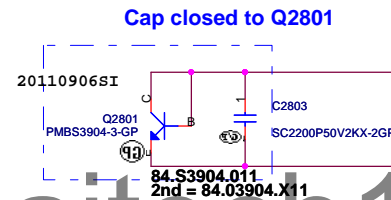
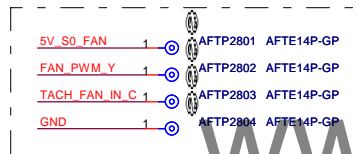
Sheet 26 of 103



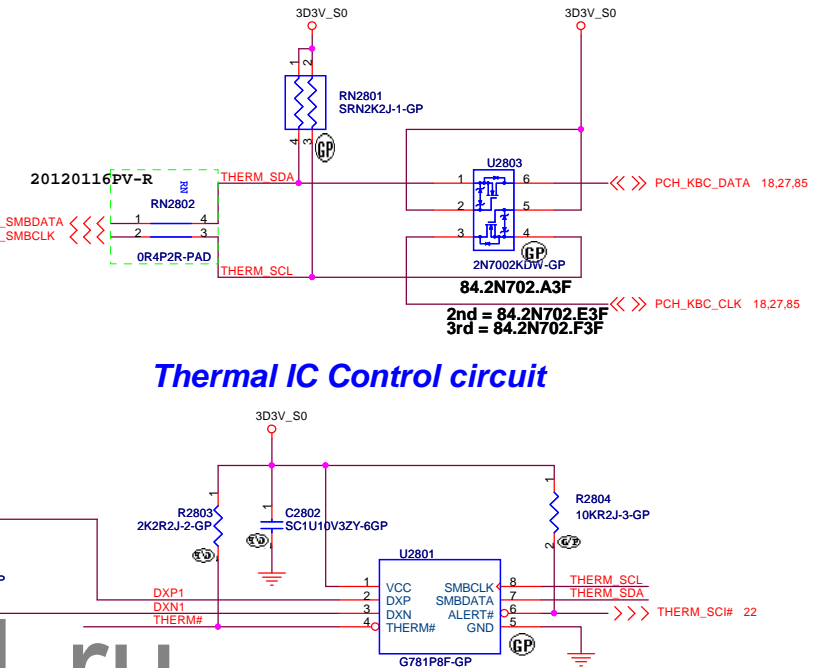
4 WIRE PWM Fan Control circuit



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

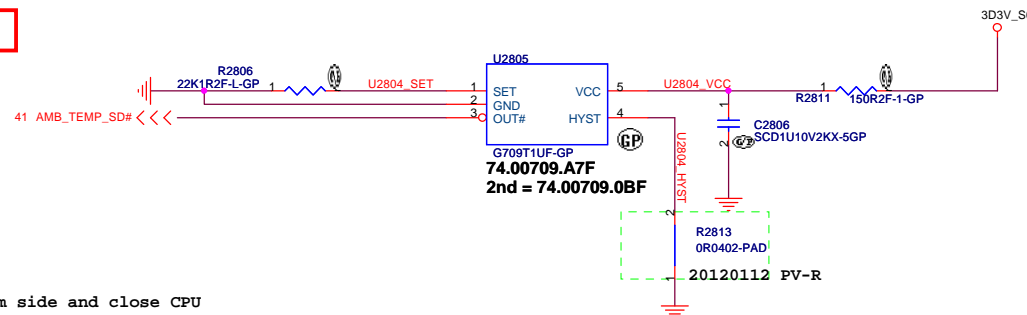


Thermal IC Control circuit



T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



Layout: PUT U2805 Bottom side and close CPU
PUT R2806 Close U2806

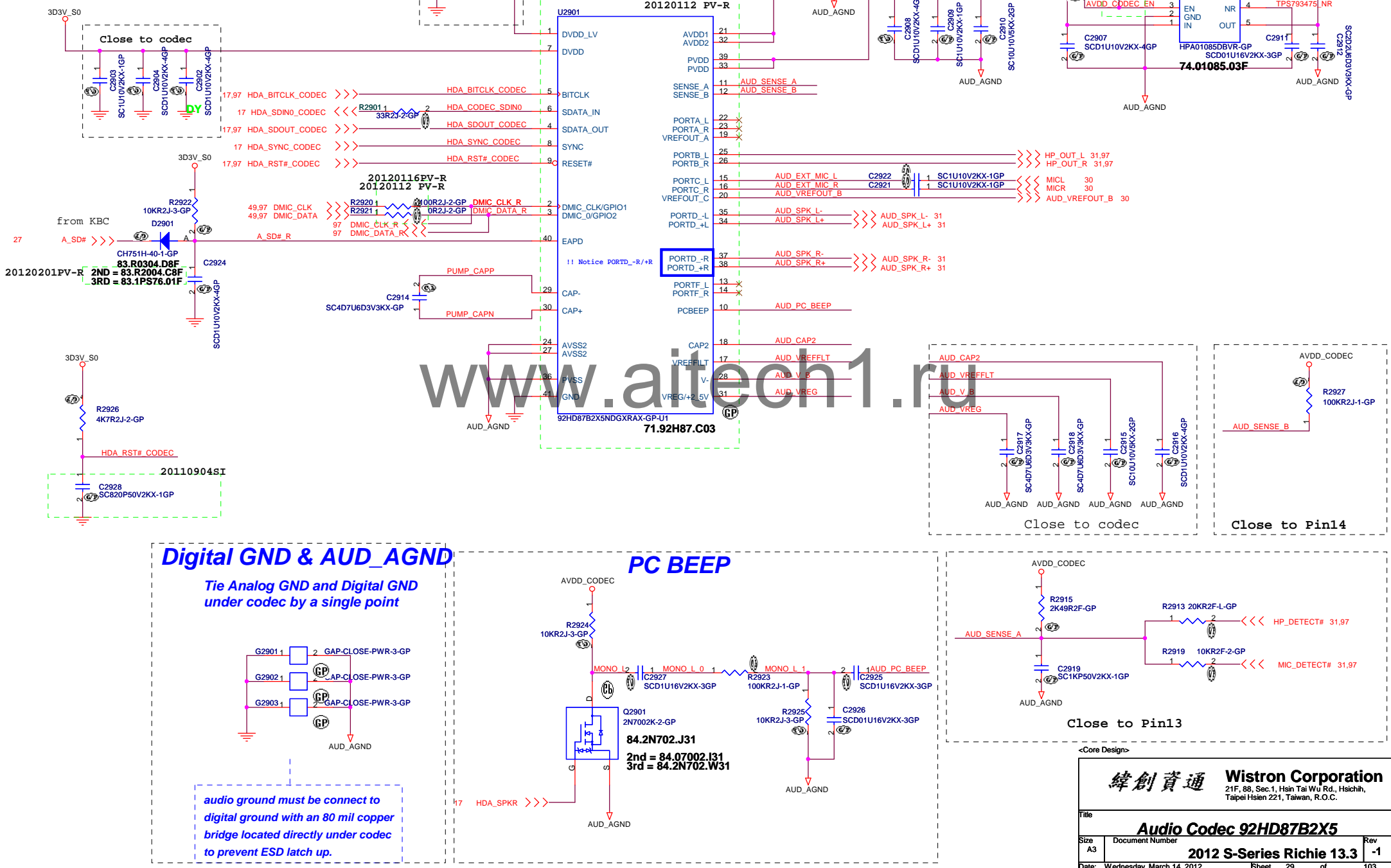
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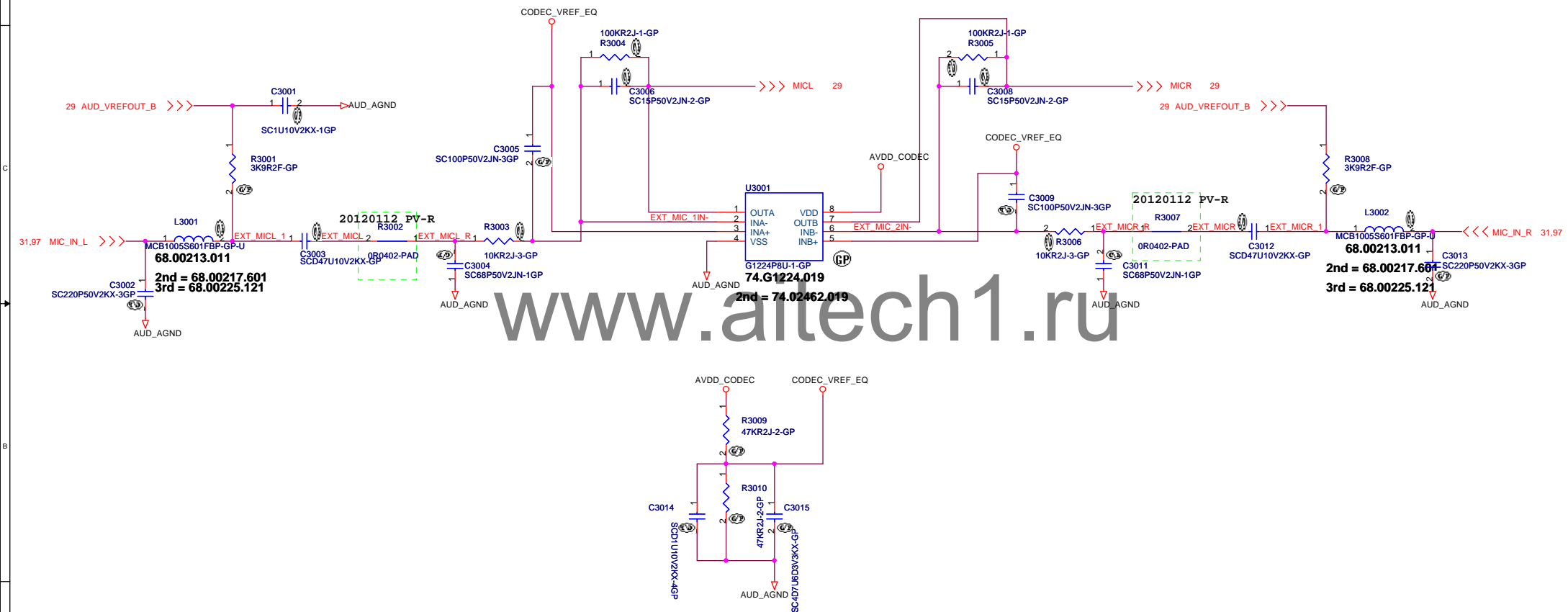
Title Thermal G781 / FAN

Size A3 Document Number 2012 S-Series Richie 13.3 Rev -1

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Pre-AMP. for External MIC

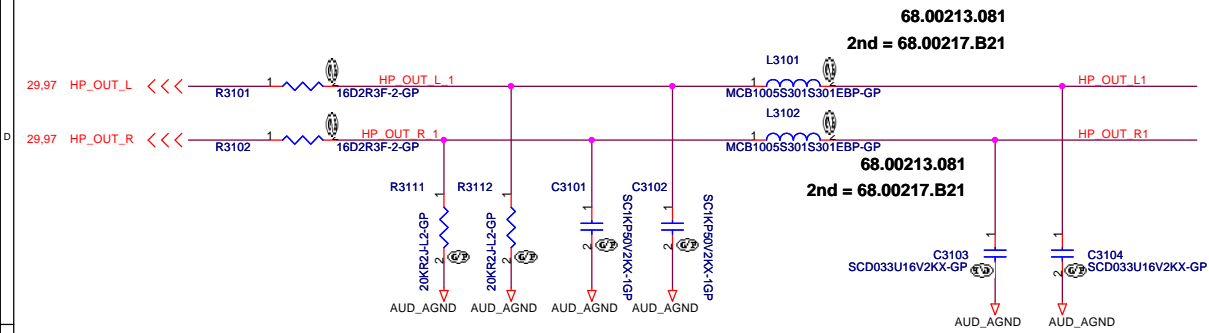


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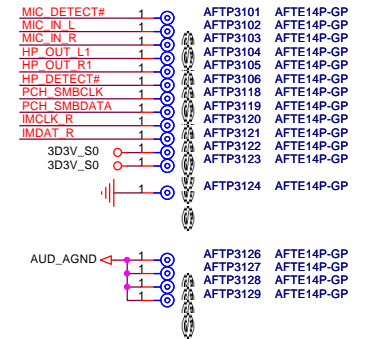
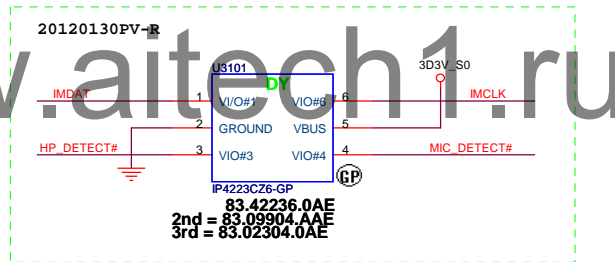
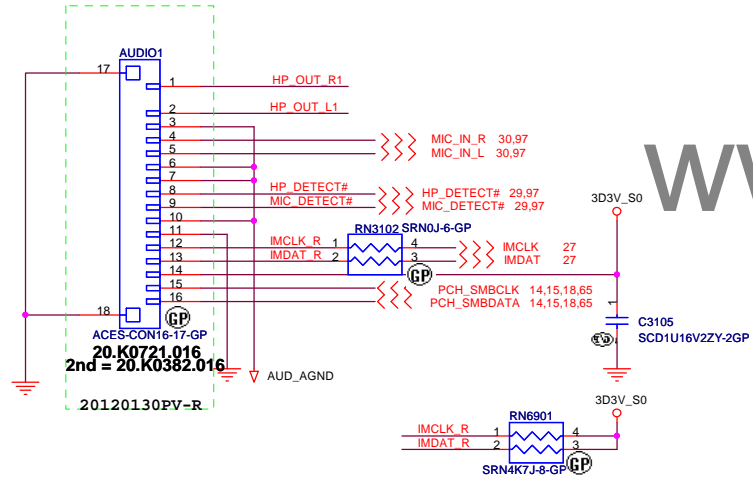
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Title			External MIC Pre-Amp	
Size	Document Number	2012 S-Series Richie 13.3		Rev
A3				-1
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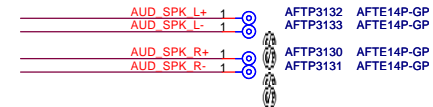
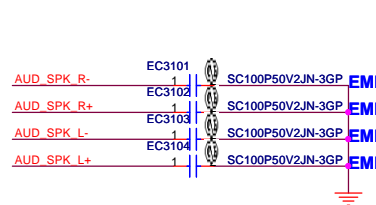
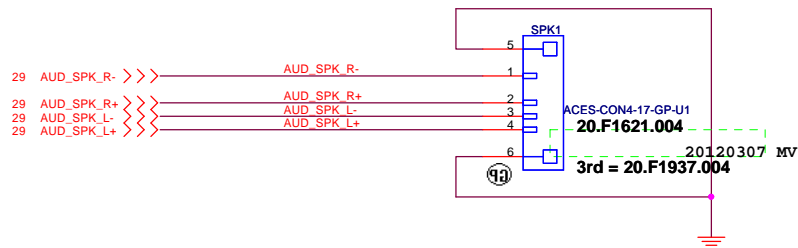
HeadPhone OUT



Audio Board +Touch Pad Connector



Speaker Connector



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Title

AUDIO Connector

Size
A

Document Number

2012 S-Series Richie 13.3

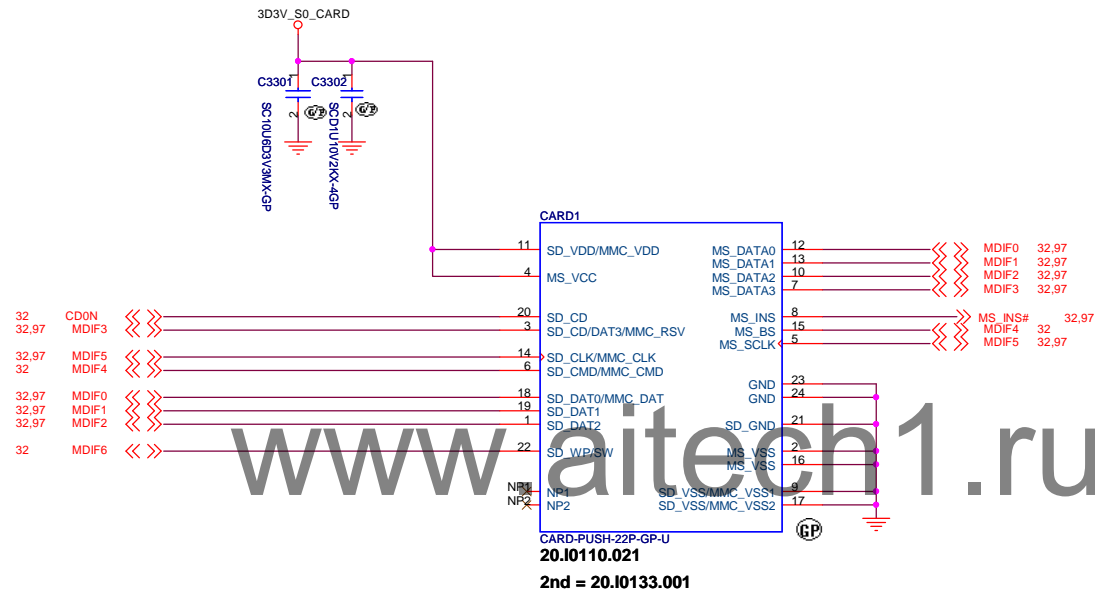
Rev
-1

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CR1_CDxN Detection Table

CR1_CDxN		Card Type
1	0	
H	H	(No Card)
H	L	SD Card/MMC
L	H	MemoryStick
L	L	XD Card



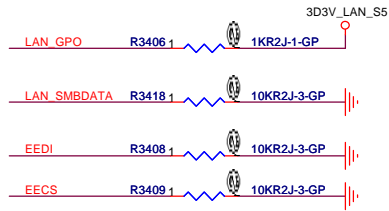
Pin Name	Default Mode	SD/MMC Card	MS Card
MDIO0	SD/MMC/MS	SD1_DAT0	MS1_DAT0
MDIO1		SD1_DAT1	MS1_DAT1
MDIO2		SD1_DAT2	MS1_DAT2
MDIO3		SD1_DAT3	MS1_DAT3
MDIO4		SD1_CMD	MS1_BS
MDIO5		SD1_CLK	MS1_CLK
MDIO6		SD1_WP	
MDIO7			
MDIO8		MMC_DAT3	MS1_DAT4
MDIO9		MMC_DAT5	MS1_DAT5
MDIO10		MMC_DAT6	MS1_DAT6
MDIO11		MMC_DAT7	MS1_DAT7
CR1_LEDN		SD1_LED#	MS1_LED#
CR1_PCTLN		SD1_PCTL#	MS1_PCTL#
CR1_CD0		SD1_CD#	
CR1_CD1			MS1_CD#

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Title			SD/MS/MMC CONNECTOR	
Size	Document Number	Rev		
A3	2012 S-Series Richie 13.3	-1		
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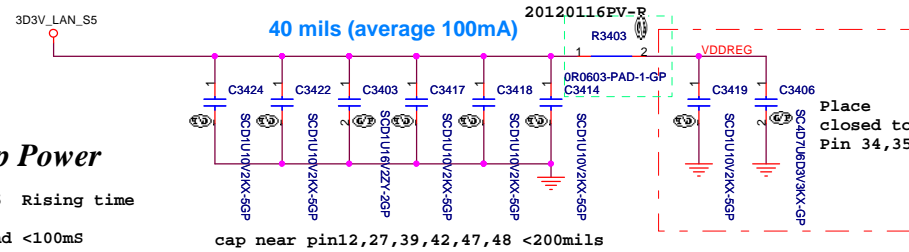
USE EFuse No ASF



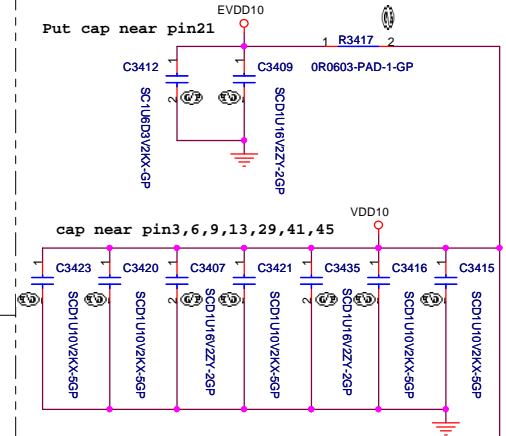
LAN CHIP-RTL8151FH

LanChip Power

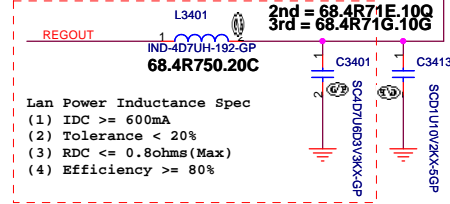
+3.3V_LAN_S5 Rising time
(10%~90%)
Spec >1ms and <100ms



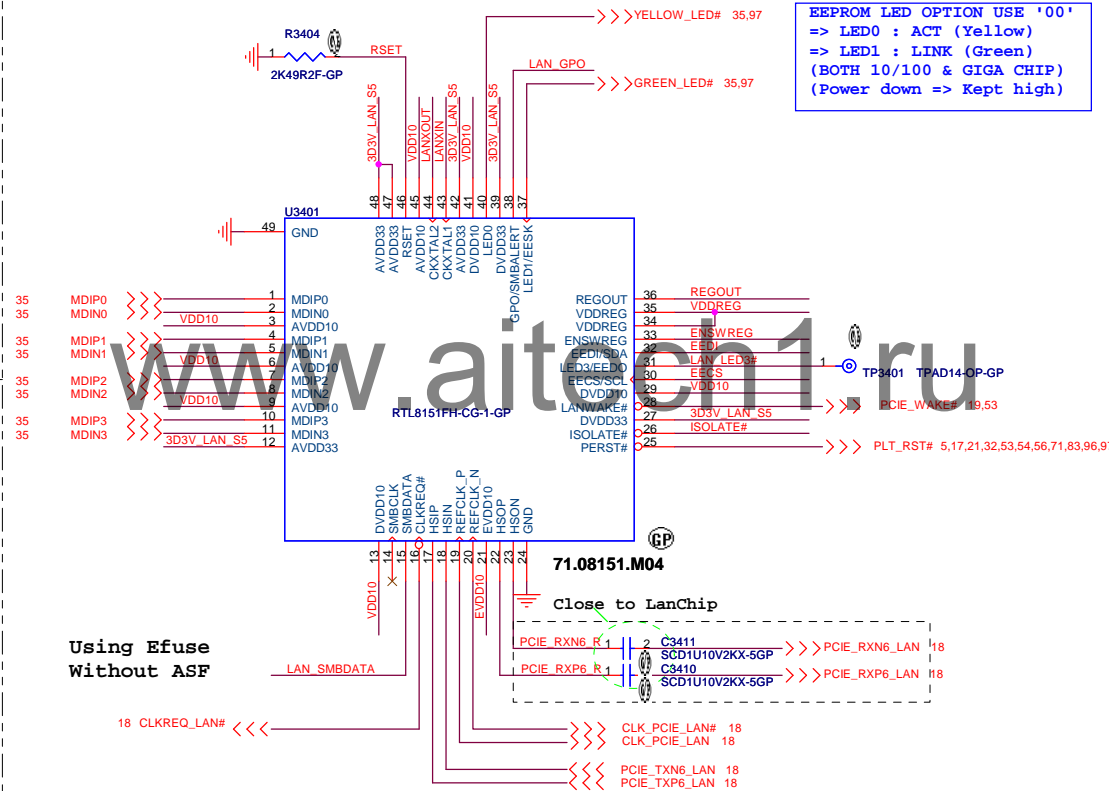
Regout power plane(1D05V)



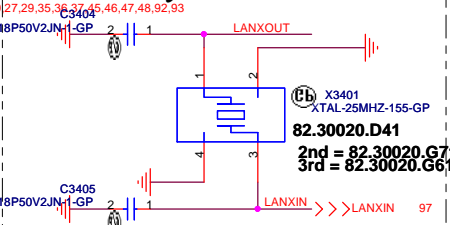
60 mils (average 300mA)



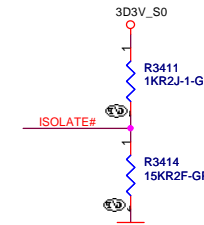
Put 4D7U L + 4D7U cap near pin36 <200mils
(2nd = 78.22610.81L)



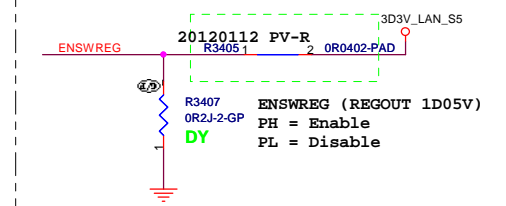
25MHz Crystal



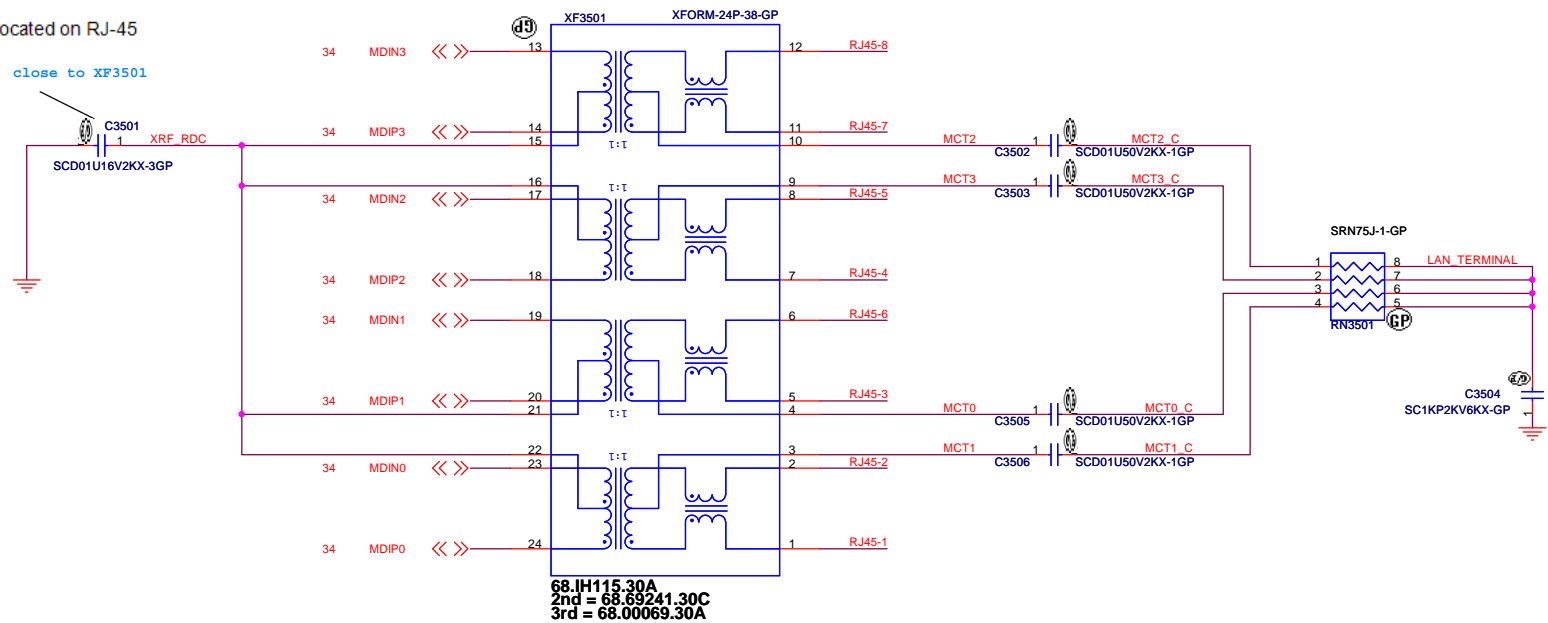
Isolate Strap Pin



Regout Switch

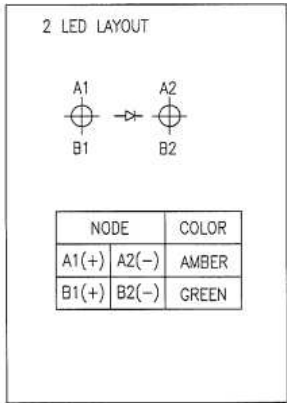
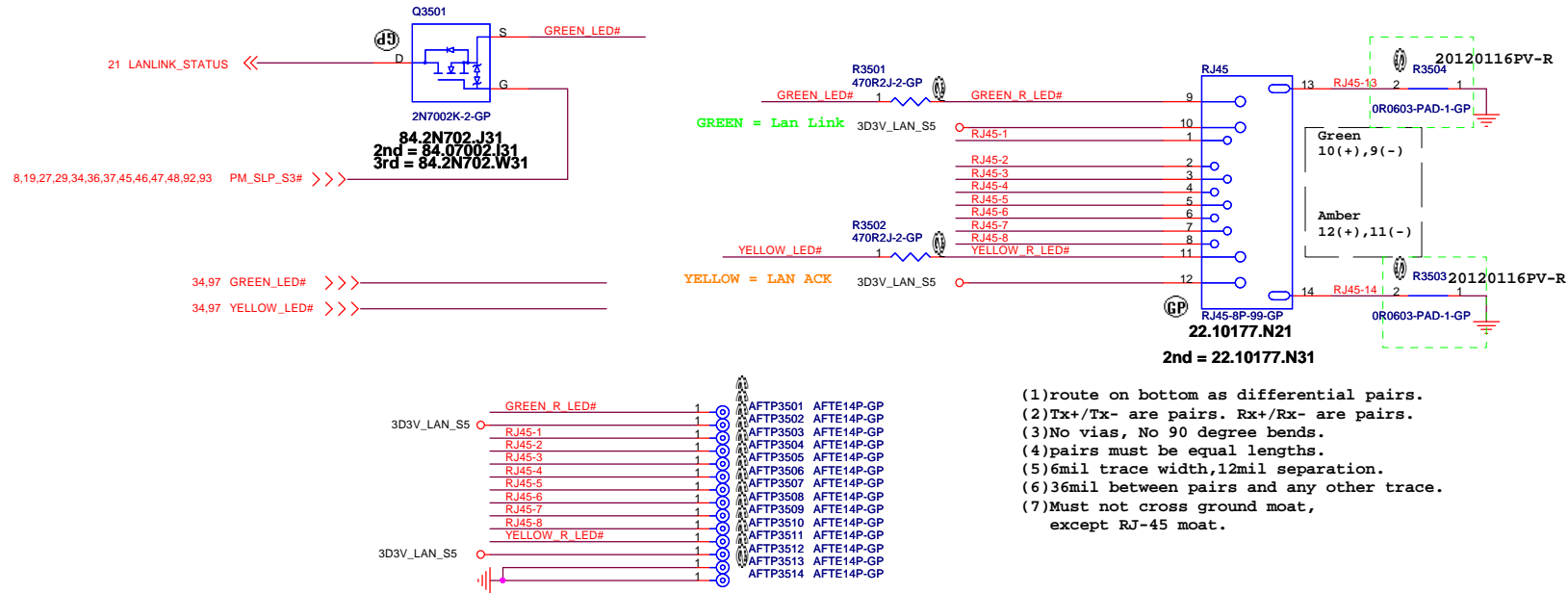


White LED for connectivity and Amber LED for activity located on RJ-45 connector



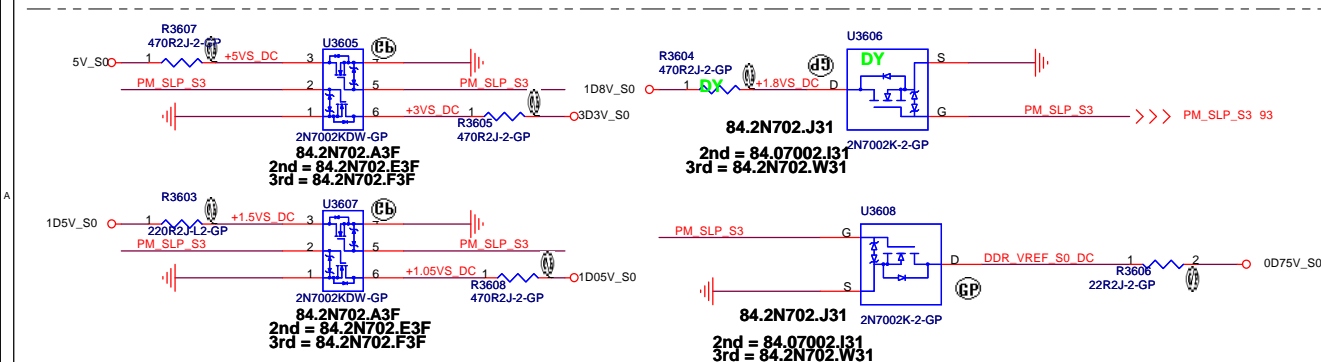
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RJ45 Connector

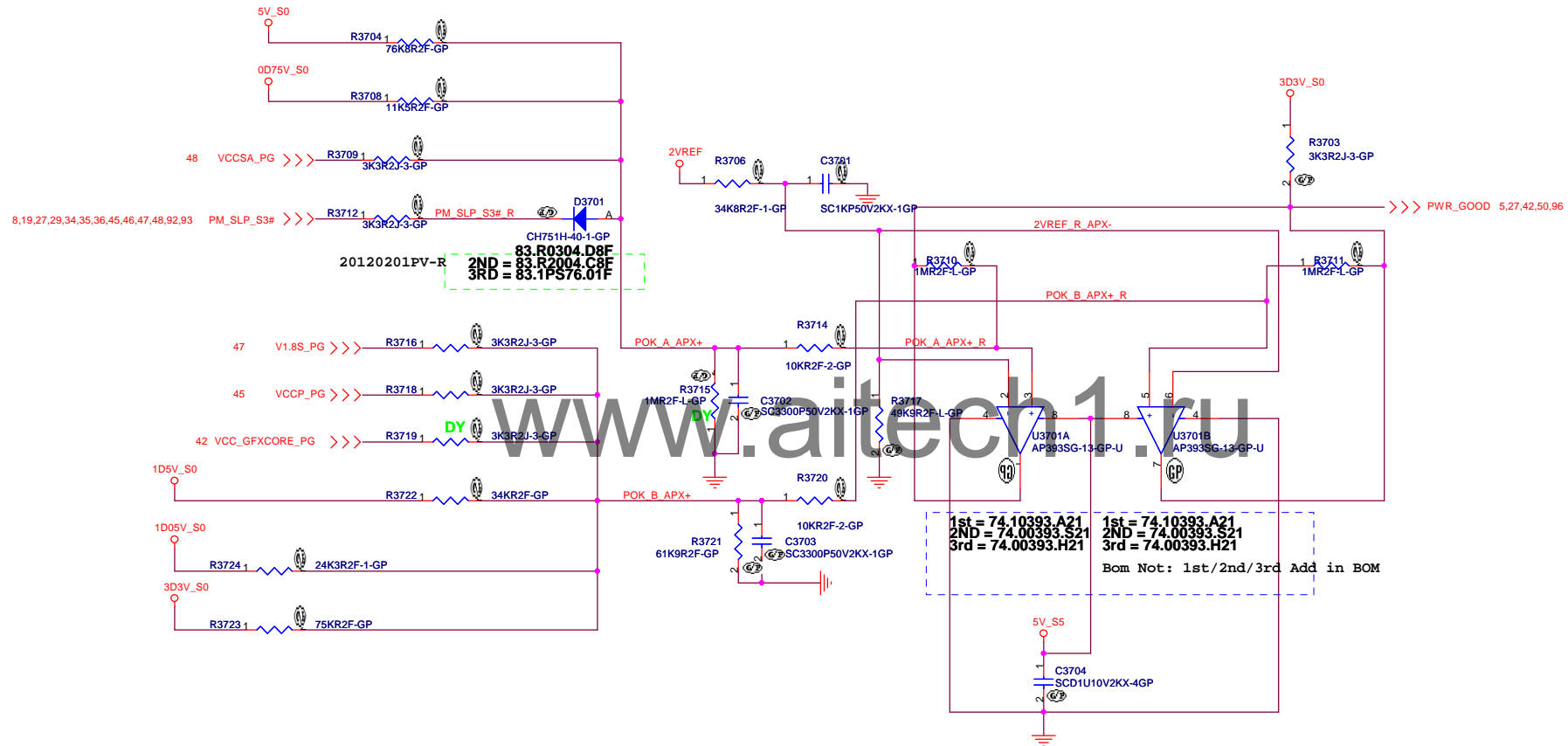


- (1)route on bottom as differential pairs.
- (2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- (3)No vias, No 90 degree bends.
- (4)pairs must be equal lengths.
- (5)6mil trace width,12mil separation.
- (6)36mil between pairs and any other trace.
- (7)Must not cross ground moat, except RJ-45 moat.

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer



POK



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No.	Title	Author	Date	Page
1	The first part of the book	John Doe	1998	100
2	The second part of the book	John Doe	1998	100
3	The third part of the book	John Doe	1998	100
4	The fourth part of the book	John Doe	1998	100
5	The fifth part of the book	John Doe	1998	100
6	The sixth part of the book	John Doe	1998	100
7	The seventh part of the book	John Doe	1998	100
8	The eighth part of the book	John Doe	1998	100
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10	The tenth part of the book	John Doe	1998	100

POK

Size
A3

Document Number

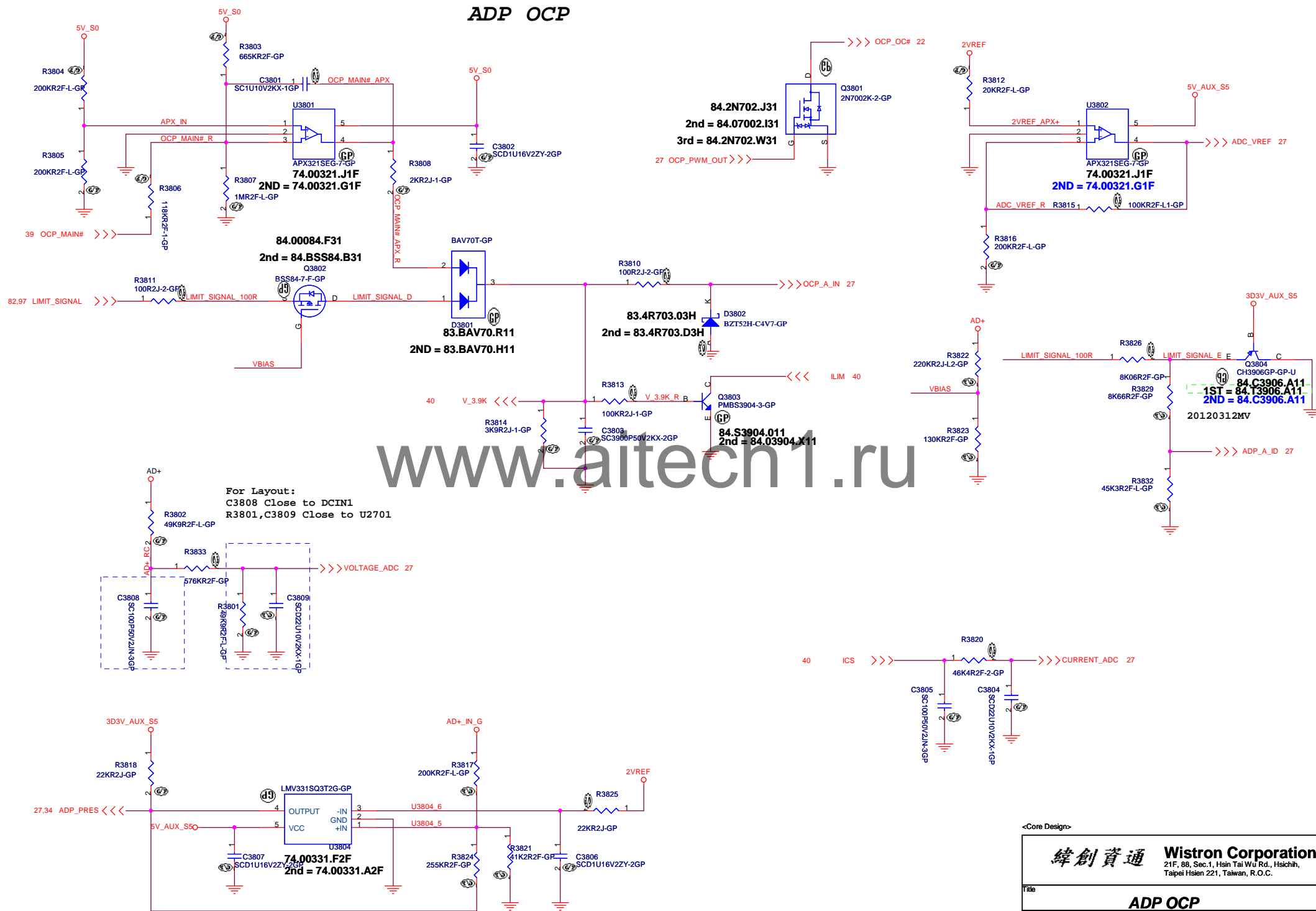
2012 S-Series Richie 13.3

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ADP OCP

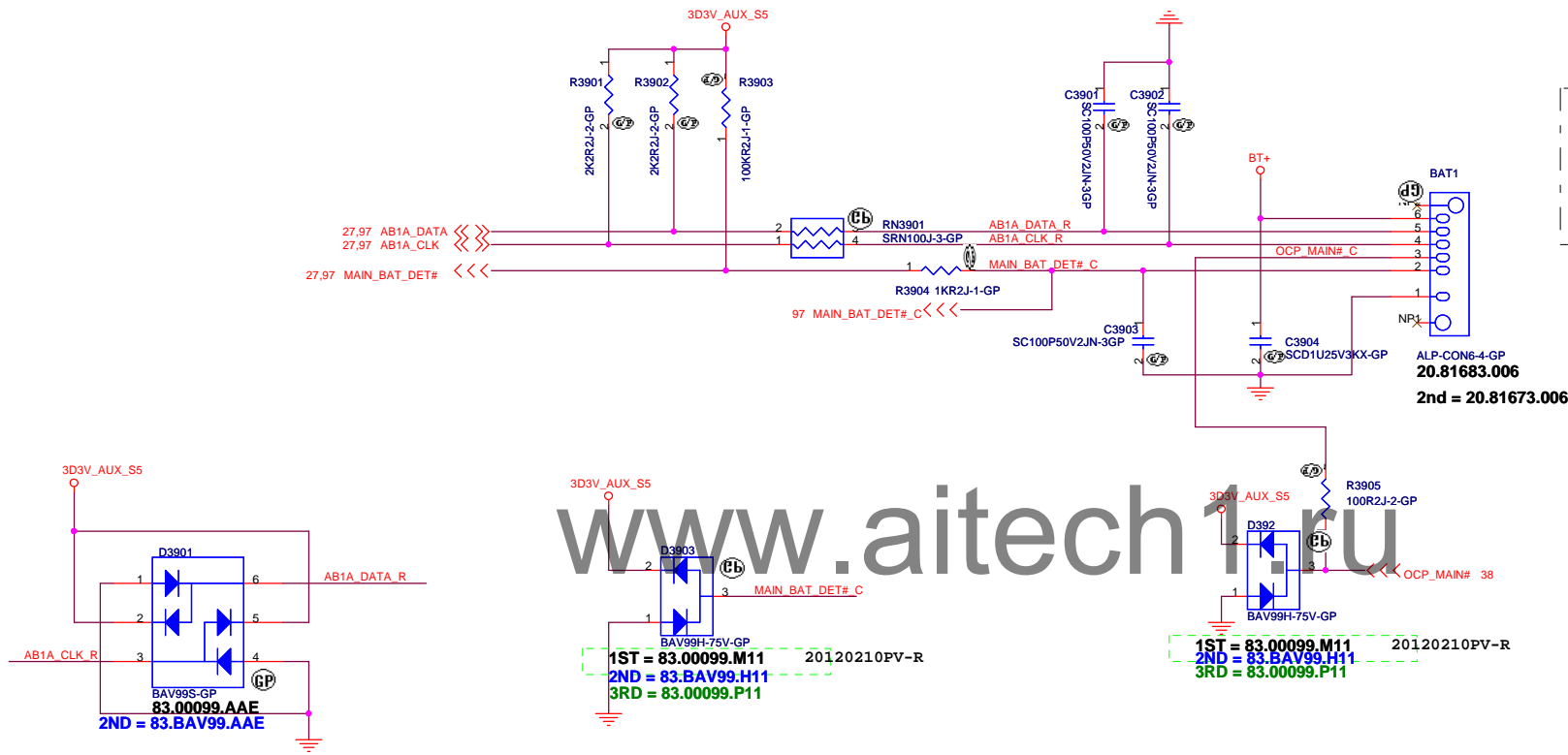


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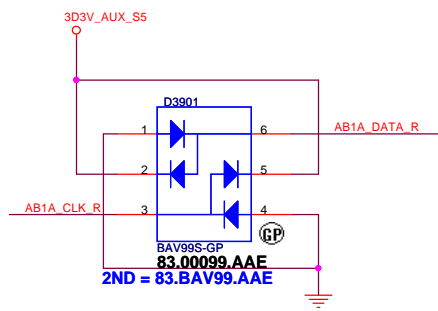
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 Taipei Hsien 221, Taiwan, R.O.C.

ADP OCP			
2012 S-Series Richie 13.3			
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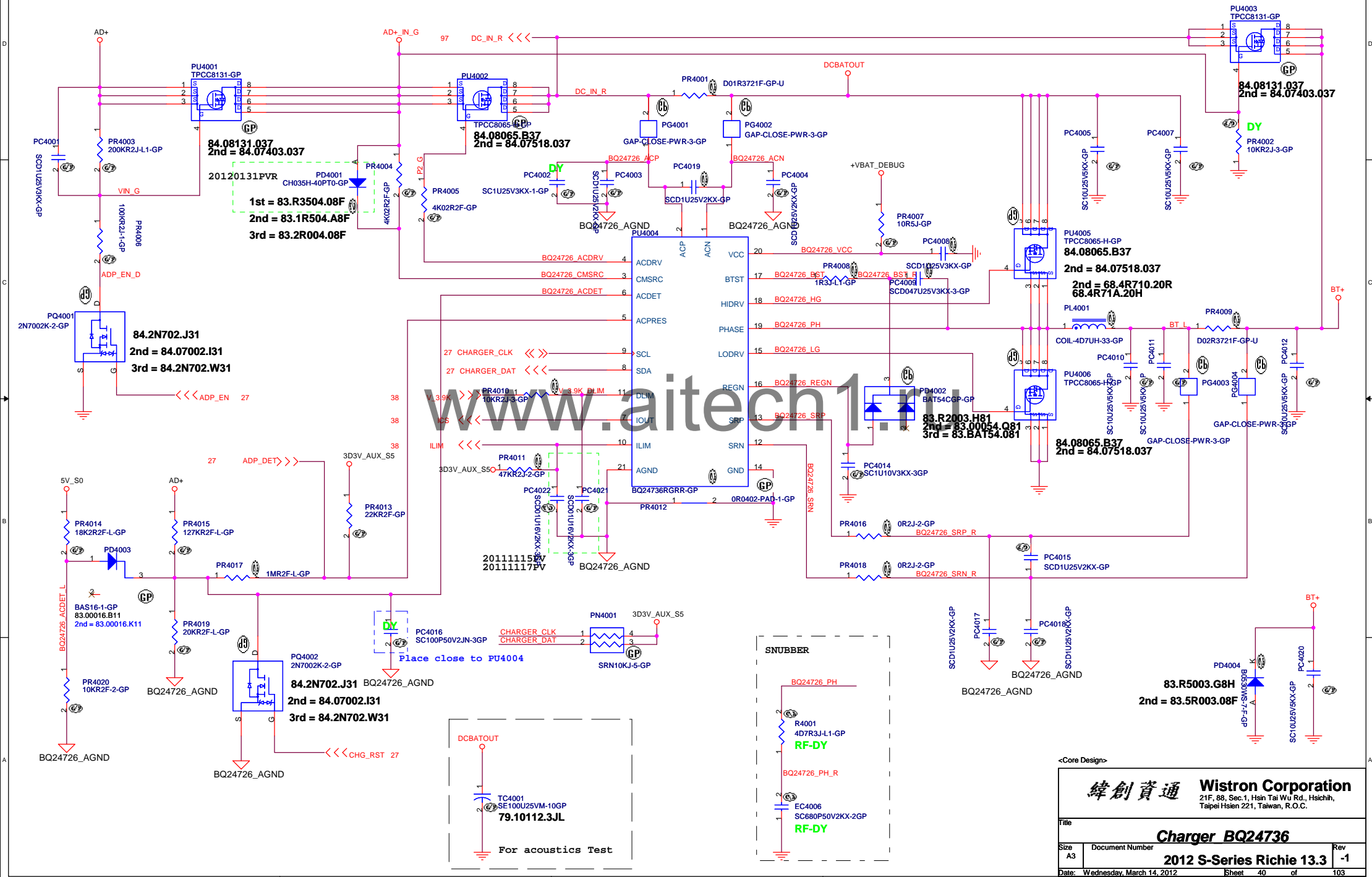
Battery Connector



BT+	1	AFTP3901	AFTE14P-GP
BT+	1	AFTP3902	AFTE14P-GP
AB1A_DATA_R	1	AFTP3903	AFTE14P-GP
AB1A_CLK_R	1	AFTP3904	AFTE14P-GP
MAIN_BAT_DET#_C	1	AFTP3905	AFTE14P-GP
OCP_MAIN#_C	1	AFTP3906	AFTE14P-GP
GND	1	AFTP3907	AFTE14P-GP
GND	1	AFTP3908	AFTE14P-GP



BQ24736 for CHARGER





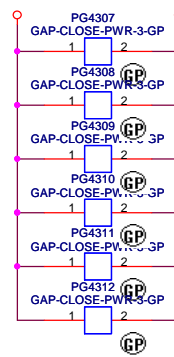
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TPS51123RGER 5V/3D3V			
Size	Document Number	Rev	
A3	2012 S-Series Richie 13.3	-1	
Date:	Saturday, March 17, 2012	Sheet	41 of 103

Route Parallel

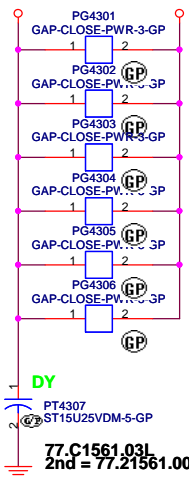


Title			
ISL95832 IMVP7-1/3			
Size A2	Document Number		Rev
	2012 S-Series Richie 13.3		-1
Date:	Wednesday, March 14, 2012		Sheet 42 of 103

DCBATOUT PWR_VCCCORE2_DCBATOUT



DCBATOUT PWR_VCCCORE1_DCBATOUT



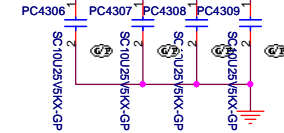
Vcc_core
Iccmax=53A
Itdc=36A
OCP>65A

42 PWR_VCORE_HG2
42 PWR_VCORE_SW2
42 PWR_VCORE_LG2

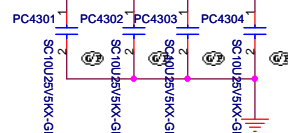
PU4303
FDMS7698-GP
84.07698.037
2nd = 84.06414.037

PU4304
FDMS0302S-GP
84.00302.037
2nd = 84.06512.037

PWR_VCCCORE2_DCBATOUT



PWR_VCCCORE1_DCBATOUT

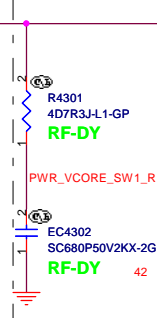


PU4301
FDMS7698-GP
84.07698.037
2nd = 84.06414.037

PU4302
FDMS0302S-GP
84.00302.037
2nd = 84.06512.037

42 PWR_VCORE_HG1
42 PWR_VCORE_SW1
42 PWR_VCORE_LG1

SNUBBER



PG4313
GAP-CLOSE-PWR

PWR_VCORE_SWN1

42

PL4301

IND-D24UH-1-GP
68.R2410.201
2nd = 68.R2610.101

PG4314

GAP-CLOSE-PWR

PWR_VCORE_SWN2

PR4271

10R2F-L-GP

PWR_VCORE_CSREF

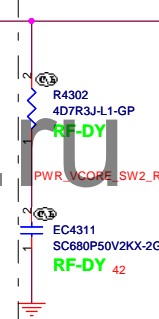
PWR_VCORE_CSREF

VCC_CORE

PT4301
ST470UF2VDM-GP
1st = 79.47719.2BL
2nd = 77.24771.13L
3rd = 79.47719.2BL

PT4303
ST470UF2VDM-GP
1st = 79.47719.2BL
2nd = 77.24771.13L
3rd = 79.47719.2BL

SNUBBER



R4302
4D7R3J-L1-GP
RF-DY

PWR_VCORE_SW2_R

EC4311
SC680P50V2KX-2GP
RF-DY 42

PWR_VCORE_SWN2

GAP-CLOSE-PWR

PG4315

GAP-CLOSE-PWR

PWR_VCORE_SWN2

PR4272

10R2F-L-GP

PWR_VCORE_CSREF

PWR_VCORE_CSREF

PWR_VCORE_CSREF

PWR_VCORE_CSREF

PWR_VCORE_CSREF

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PWR_VCORE_CSREF

PWR_VCORE_CSREF

PWR_VCORE_CSREF

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ISL95832 IMVP7-2/3

Size

Document Number

2012 S-Series Richie 13.3

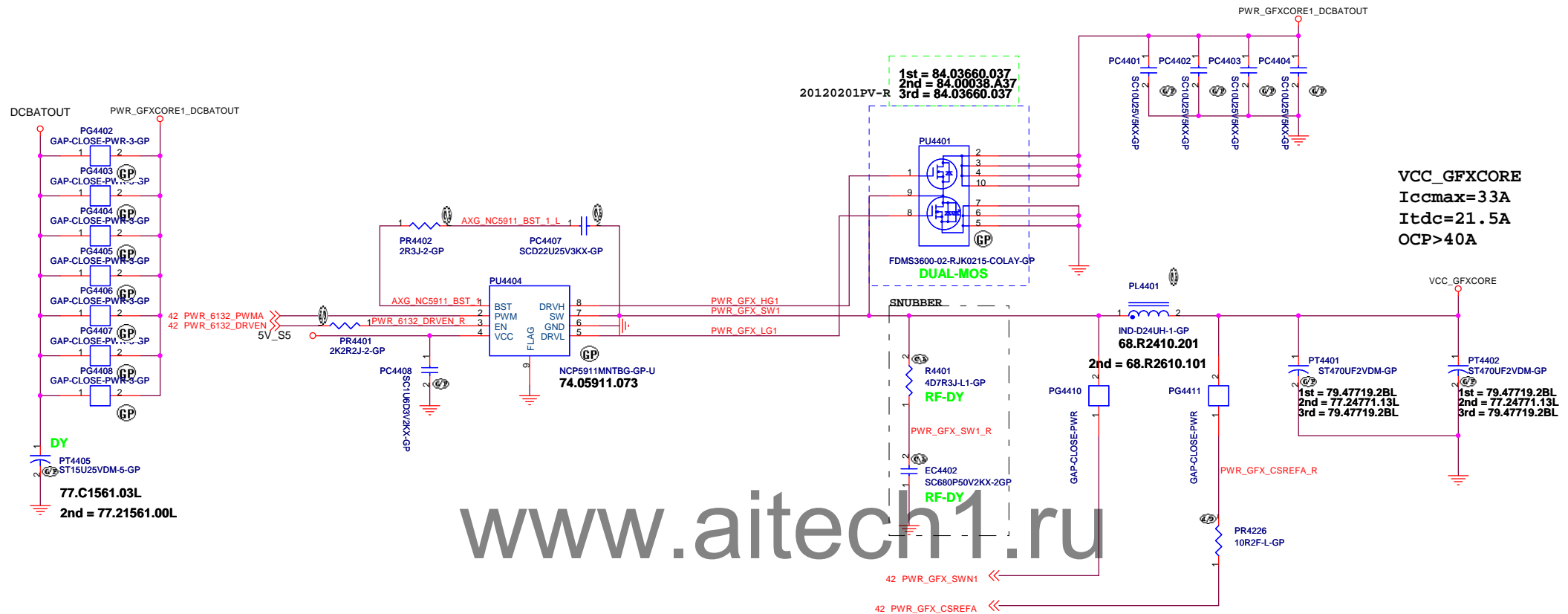
Rev

A3

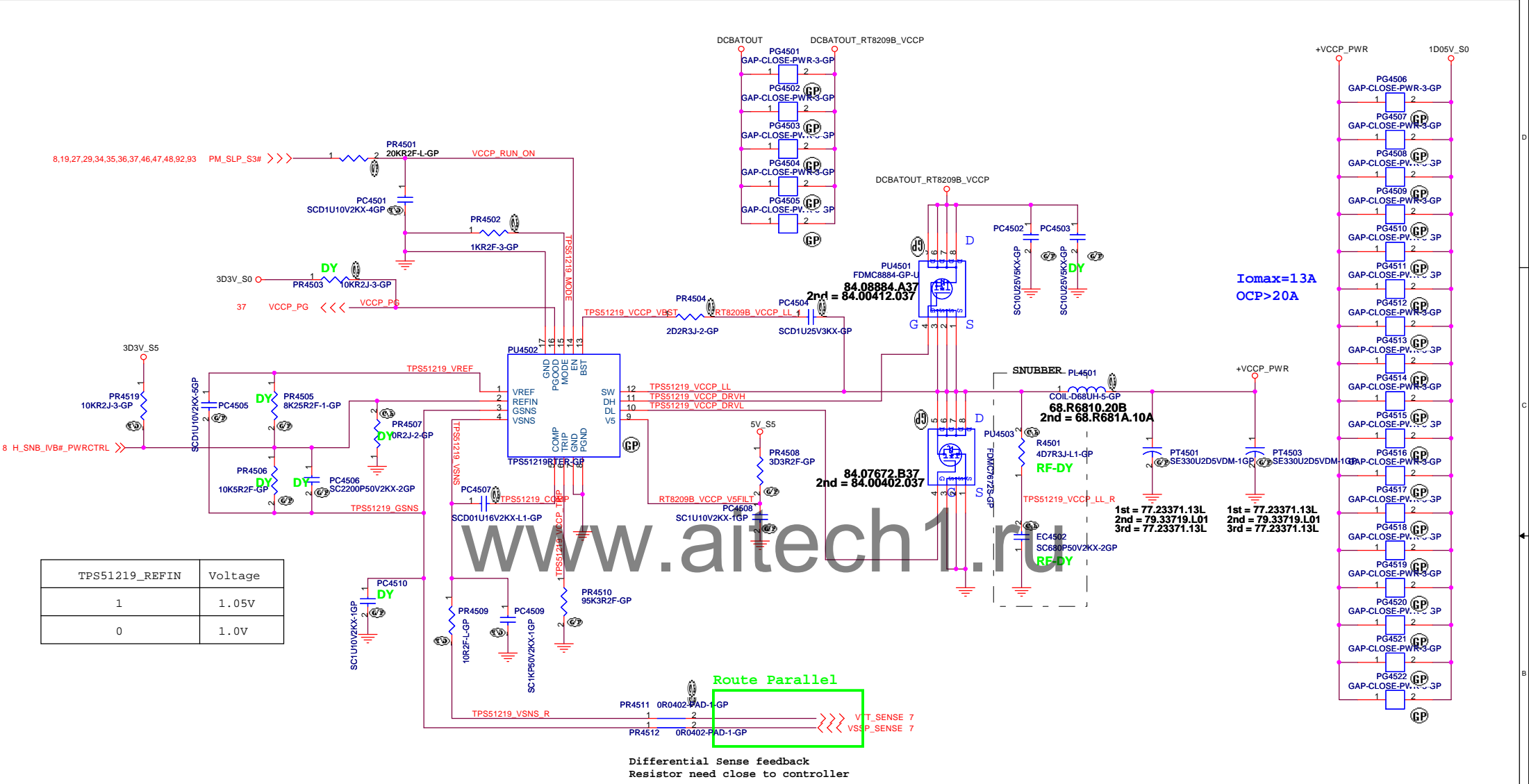
Date: Wednesday, March 14, 2012

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VCC_GFXCORE
 $I_{ccmax} = 3.3A$
 $I_{tdc} = 21.5A$
 $OCP > 40A$



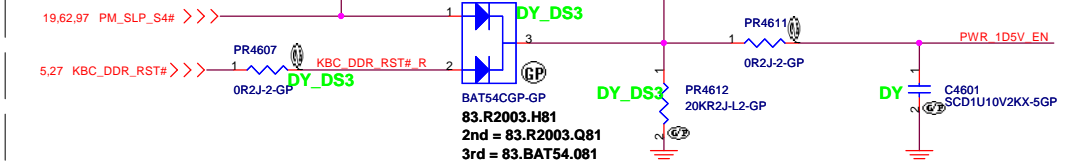
8.19.27.29.34.35.36.37.46.47.48.92.93 PM_SLP_S3# >>>

8 H_SNB_IVB#_PWRCTRL >>>

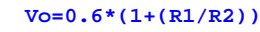
TPS51218_REFIN	Voltage
1	1.05V
0	1.0V

Route Parallel

Differential Sense feedback
Resistor need close to controller

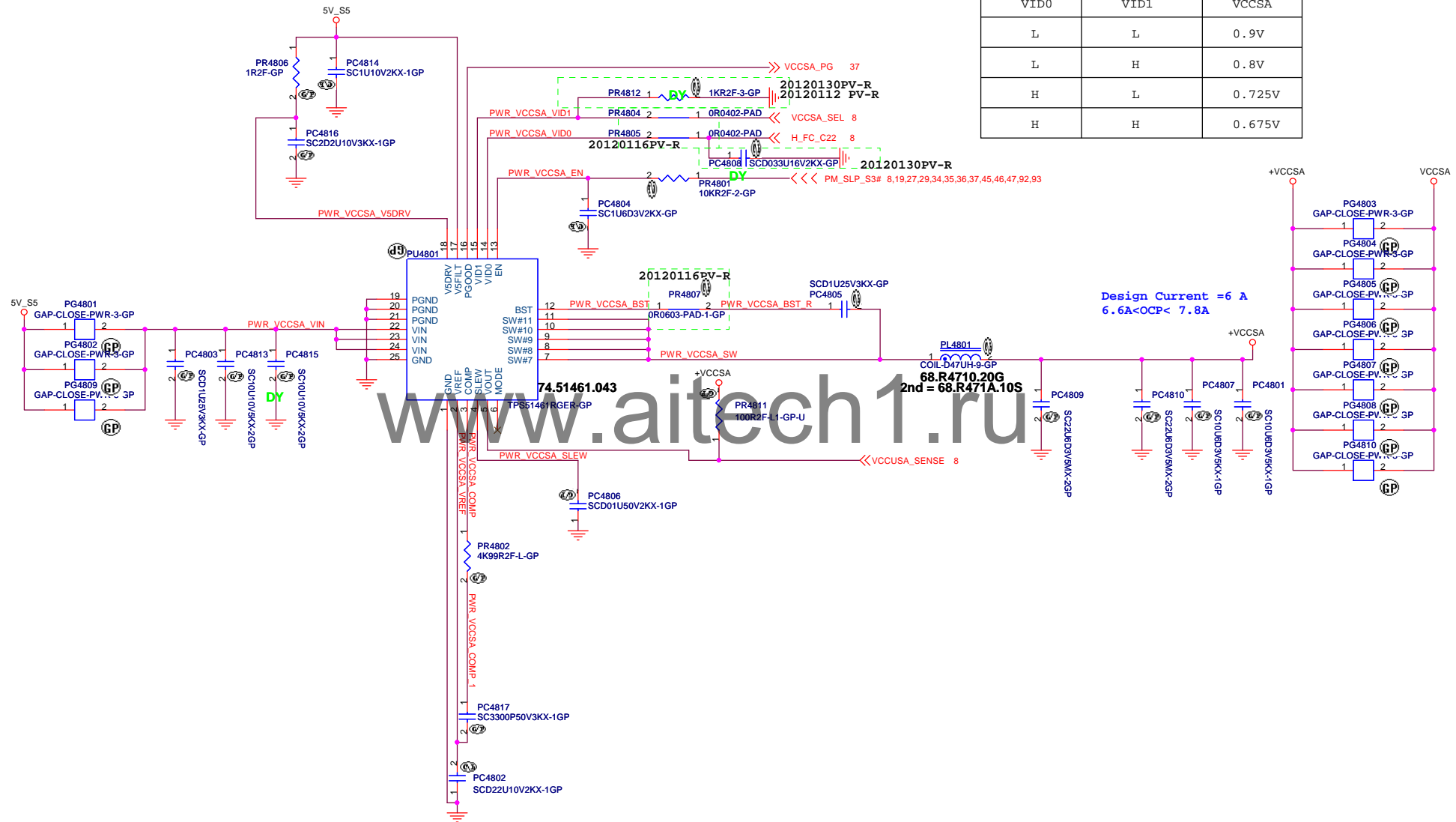


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TPS51461 for VCCSA

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



<Core Design>

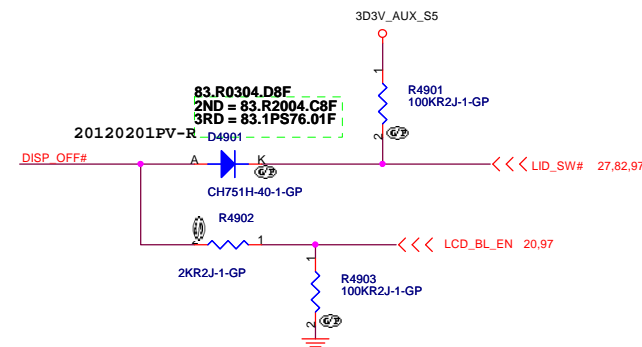
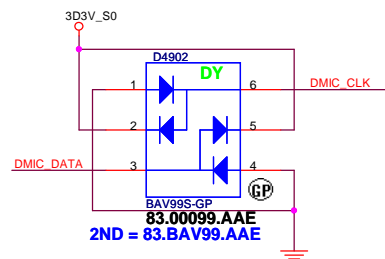
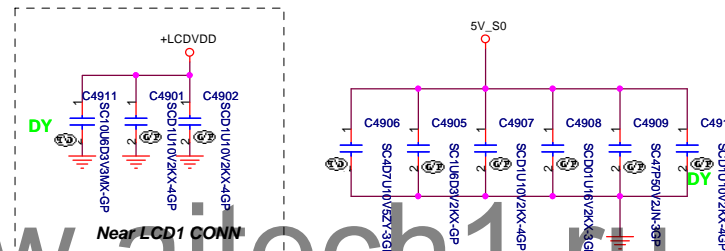
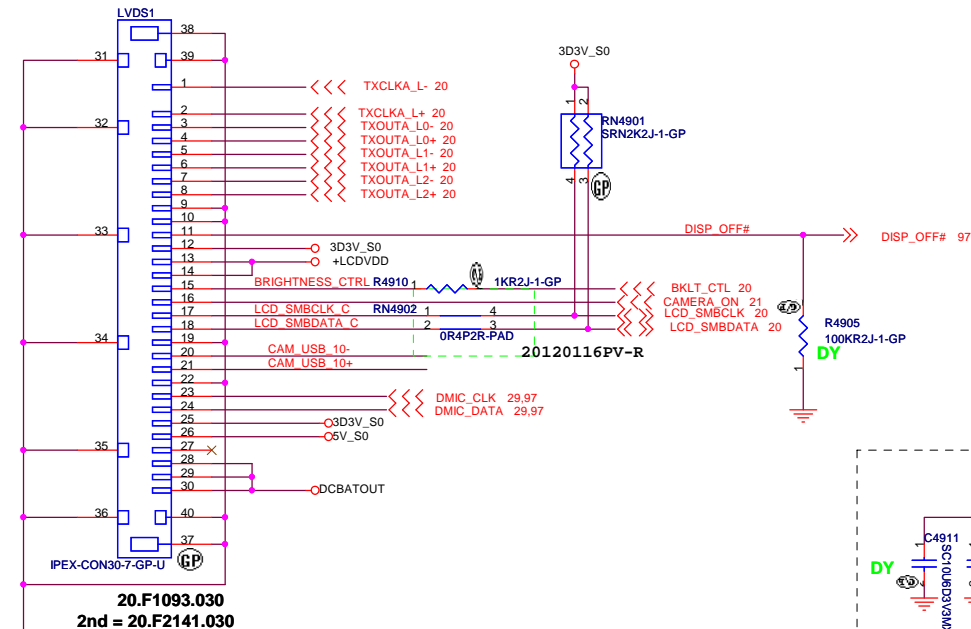
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

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ISL95870A VCCSA			
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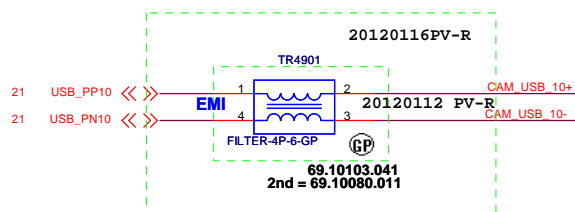
LCD Connector

CARMER PINDEFINE

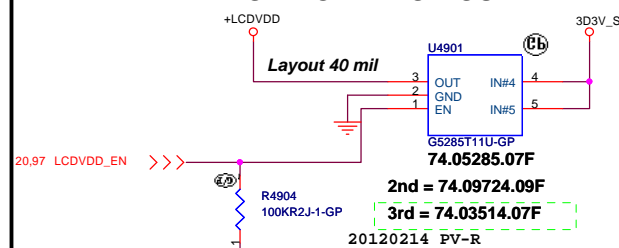
No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-



CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER

<Core Design>

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Title

LCD Connector

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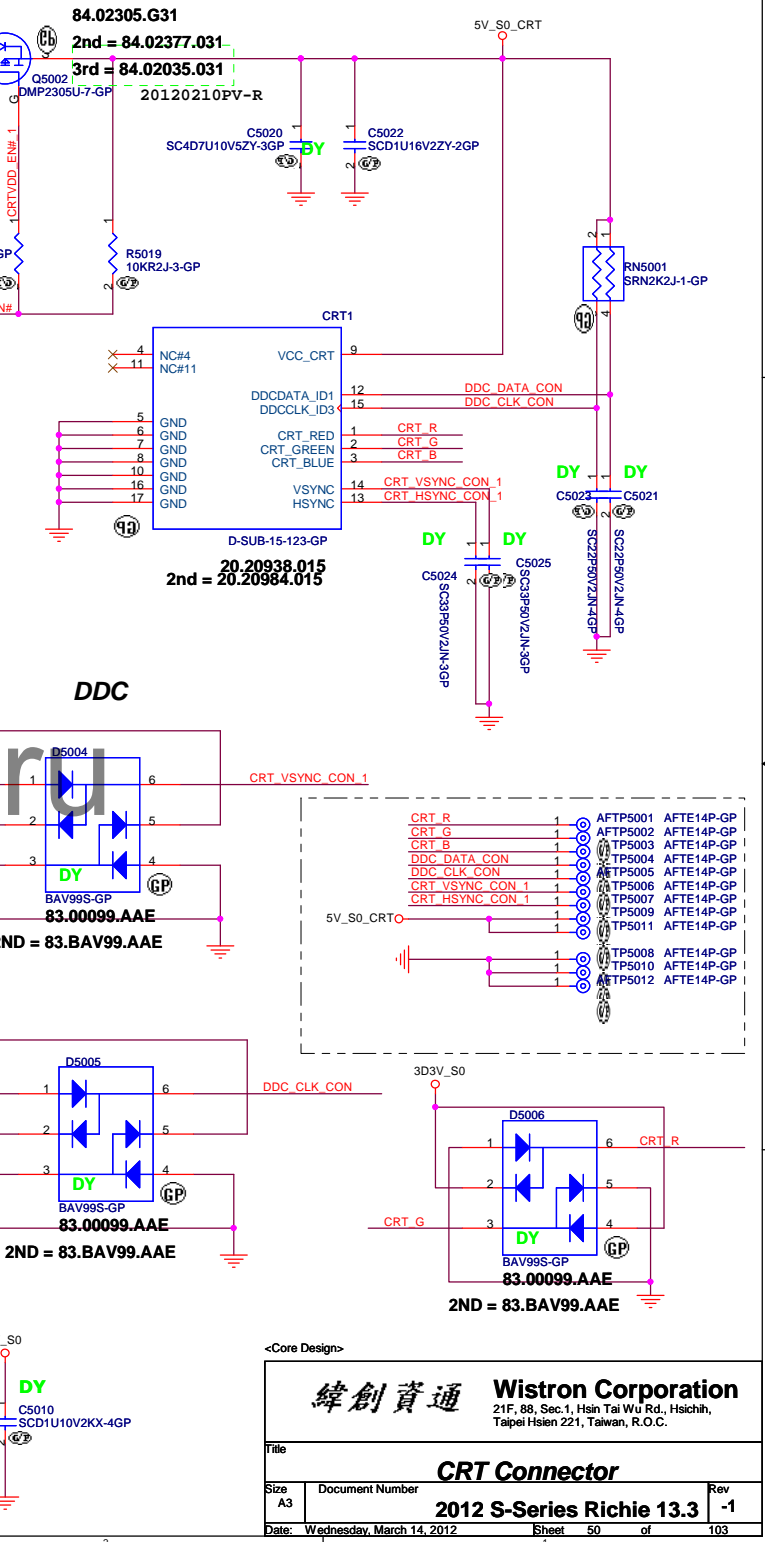
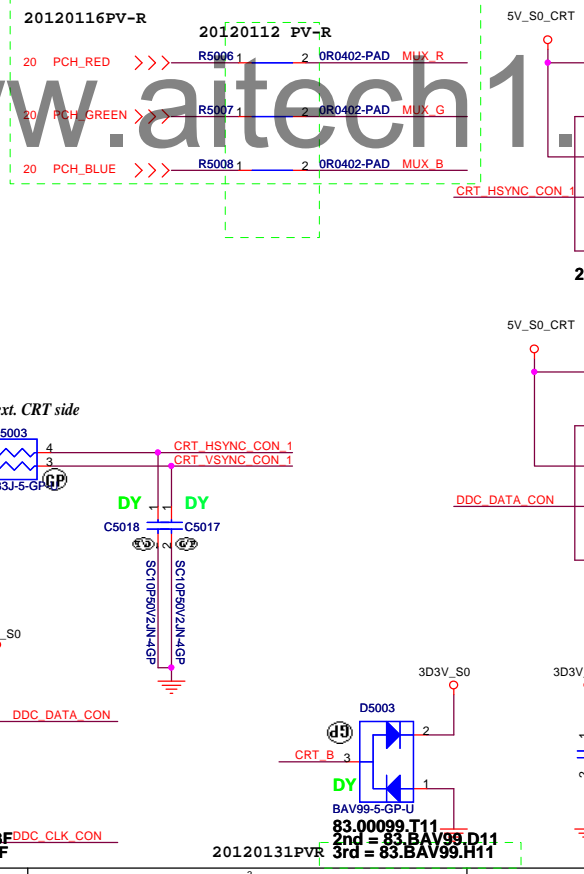
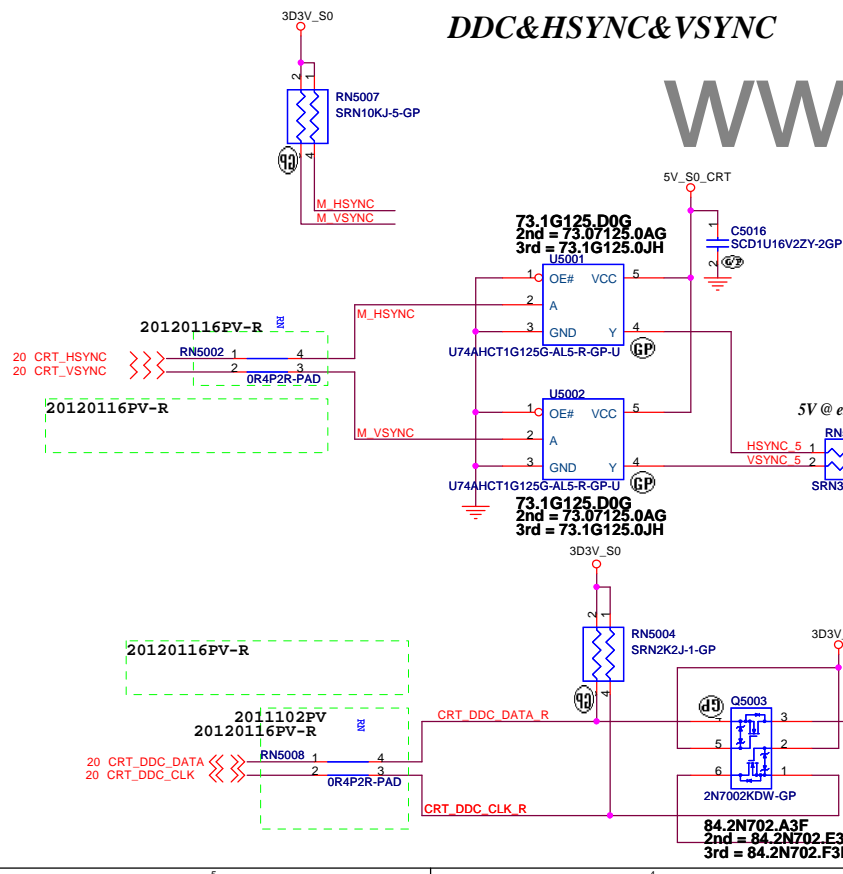
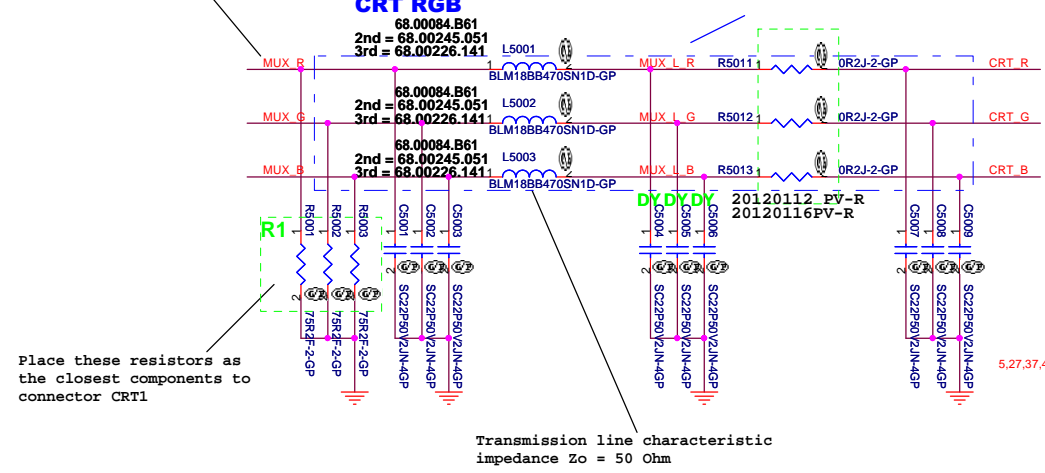
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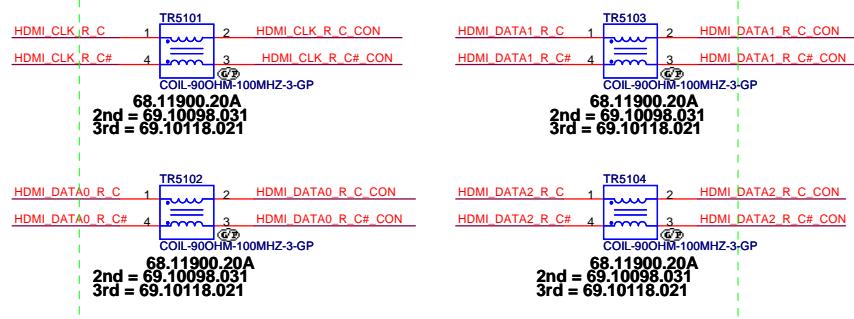
CRT Connector

CRT1
Transmission line
characteristic
impedance for RGB
signals $Z_0 = 37.5 \text{ Ohm}$

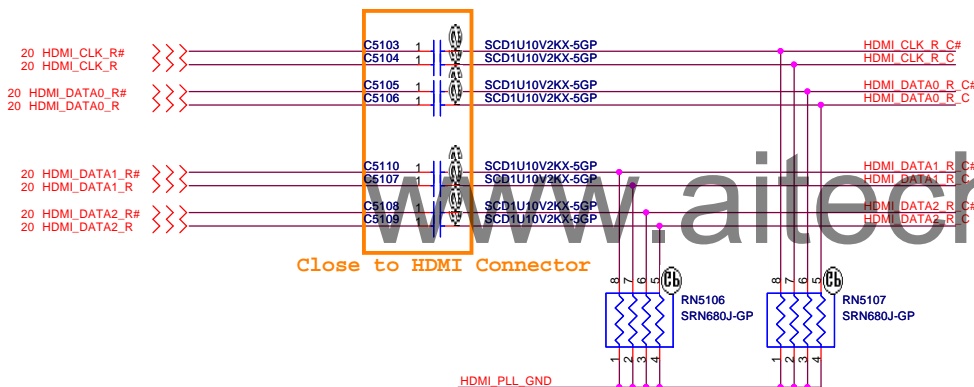


HDMI Connector

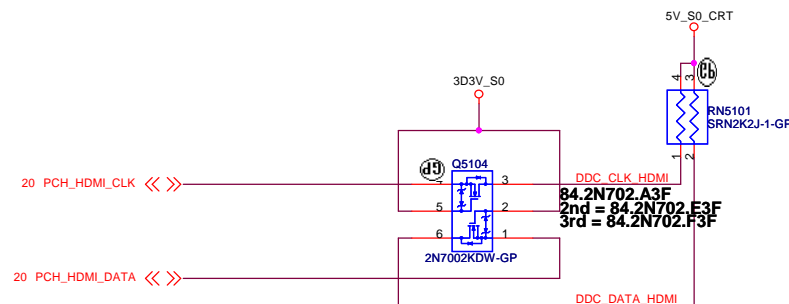
20120130PV-R



Close to PCH



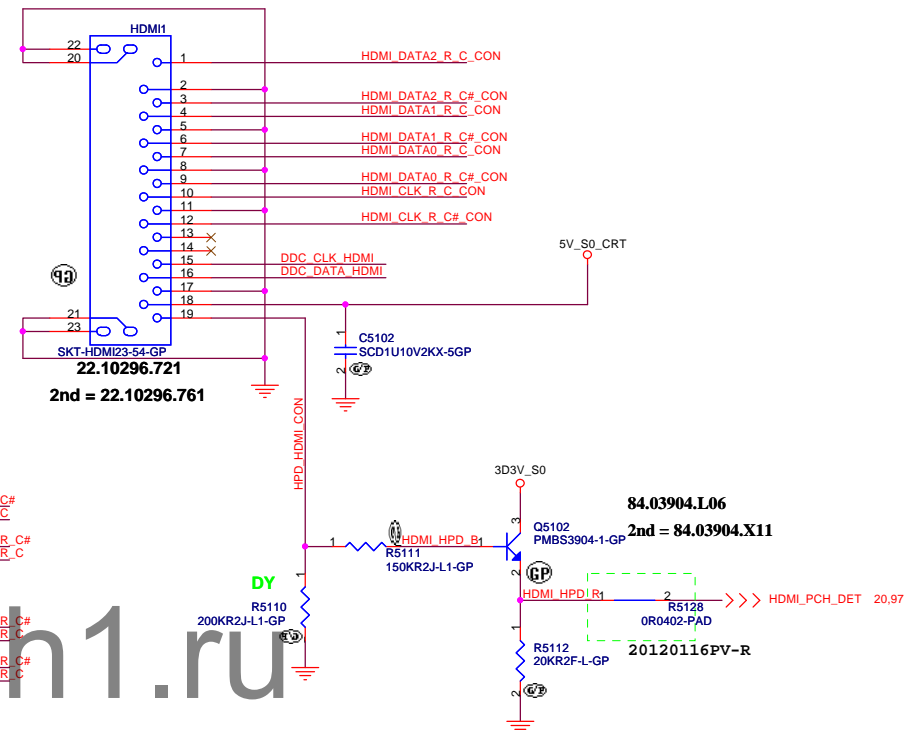
Close to HDMI Connector



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

HDMI CONN



<Core Design>

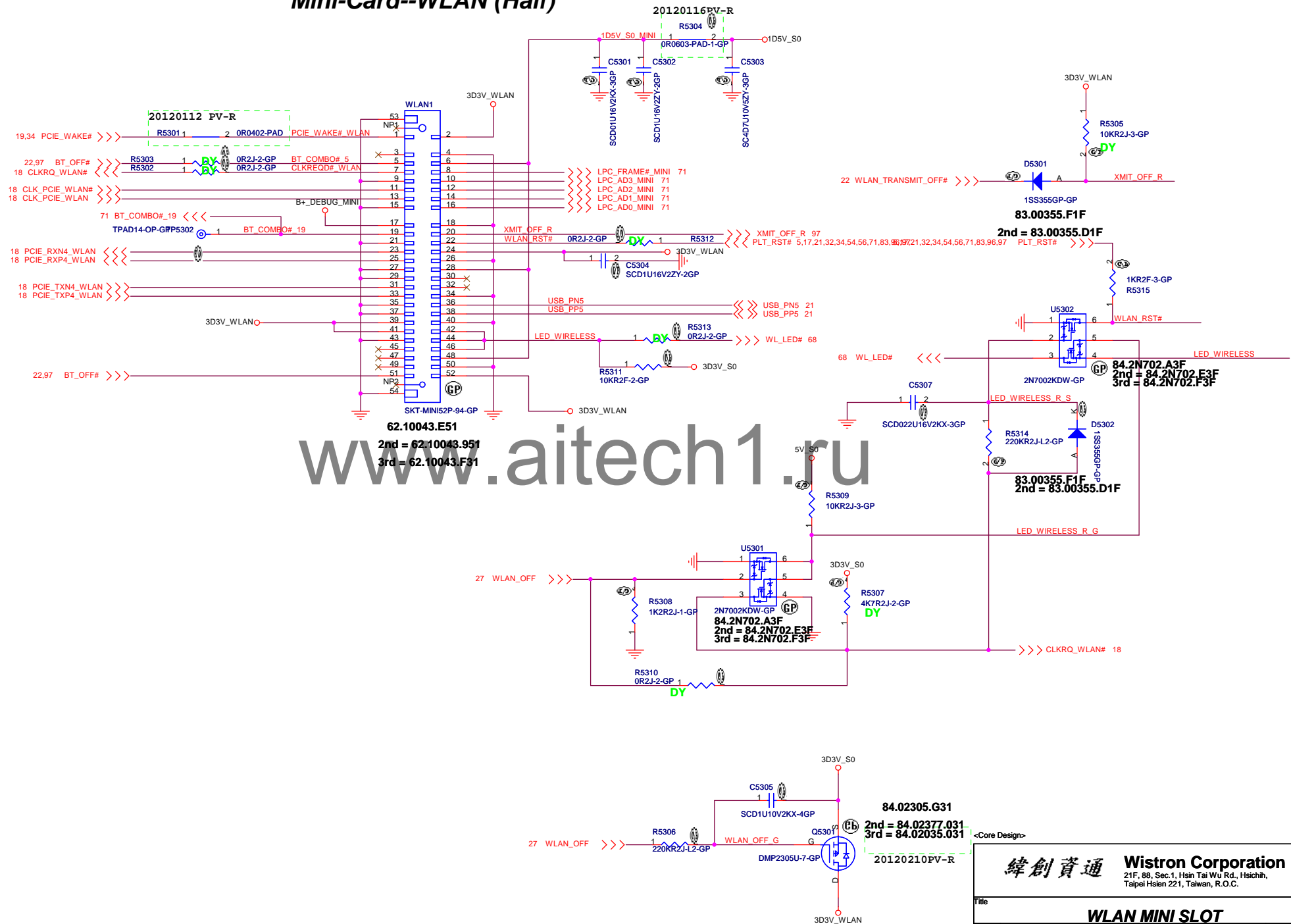
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HDMI Level Shifter/Conn		
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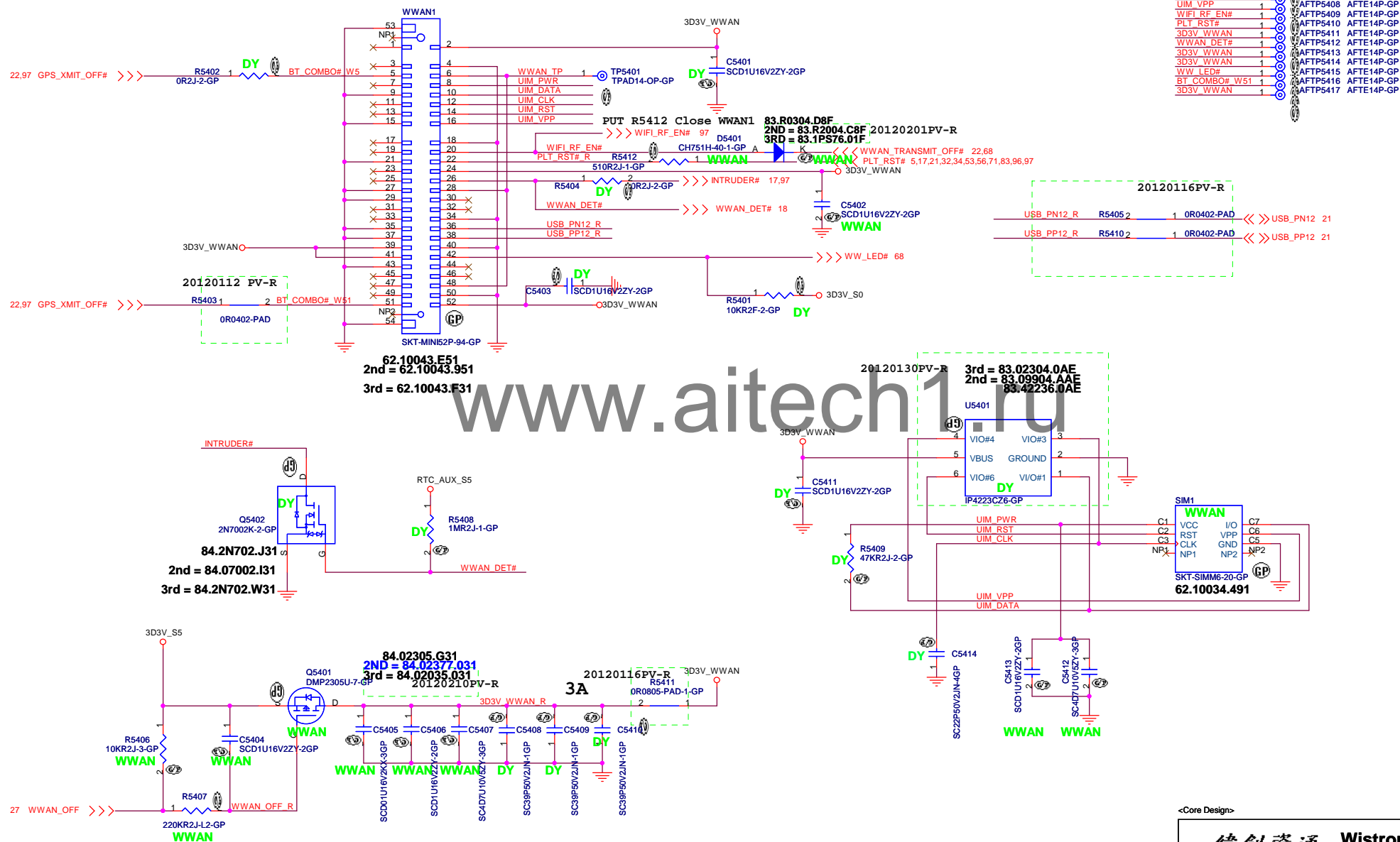
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Mini-Card--WLAN (Half)



Mini-Card--WWAN



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Title

WWAN MINI SLOT/SIM

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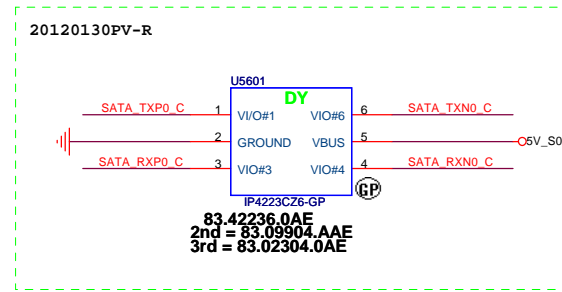
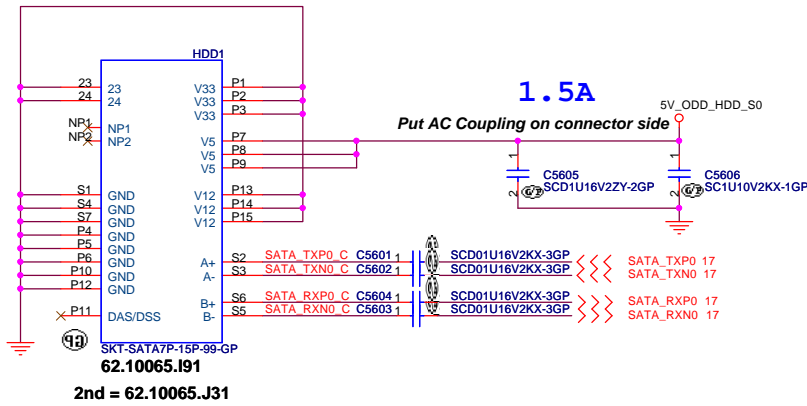
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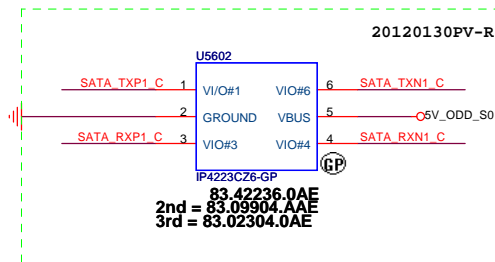
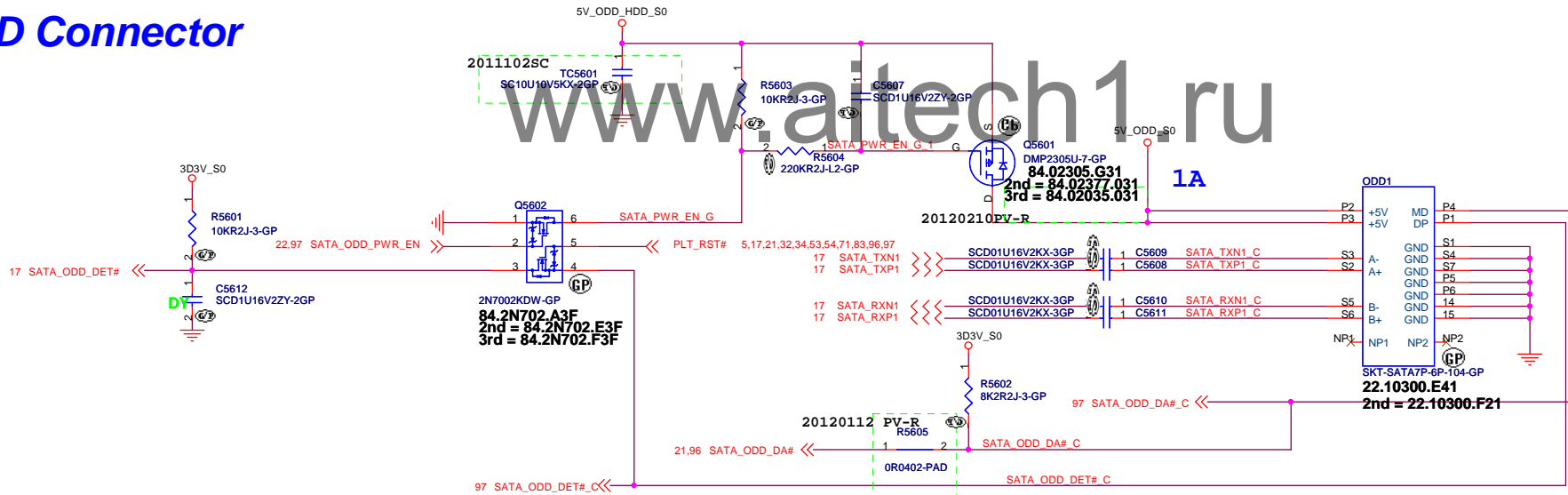
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HDD Connector



ODD Connector



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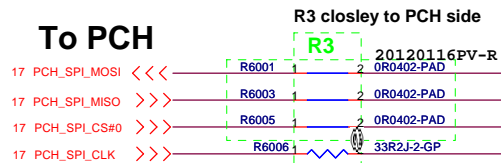
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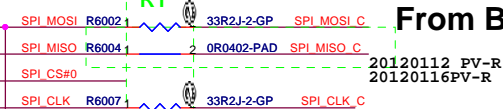
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SSID = Flash.ROM

To PCH

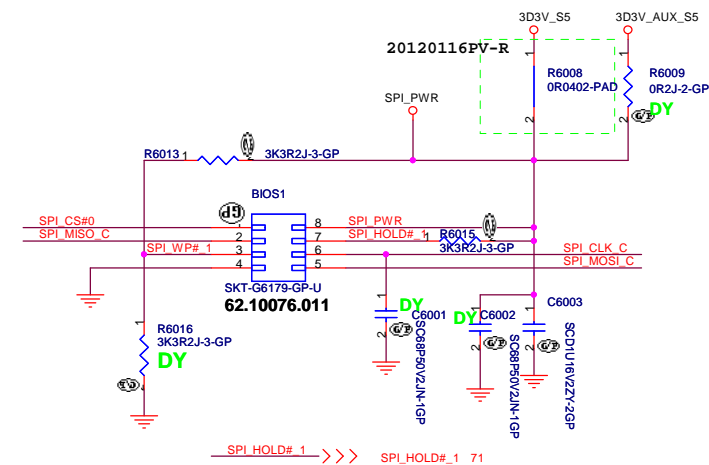


R1 closley to SPI ROM side

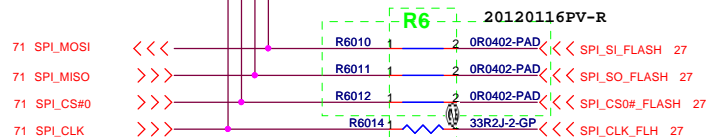


From BIOS

SYSTEM SPI ROM Socket

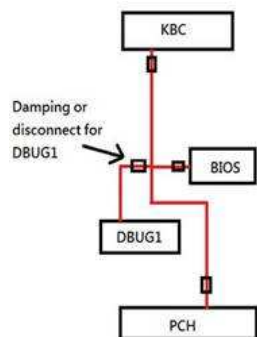


From KBC



R6 closley to KBC side

SPI Layout Note



NOTE: SPI signal use GND reference

SPI ROM PART

72.25Q64.F01	W25Q64FVSSIG	WINBOND
72.25Q64.D01	N25Q064A13ESE40F	NUMONYX

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Flash

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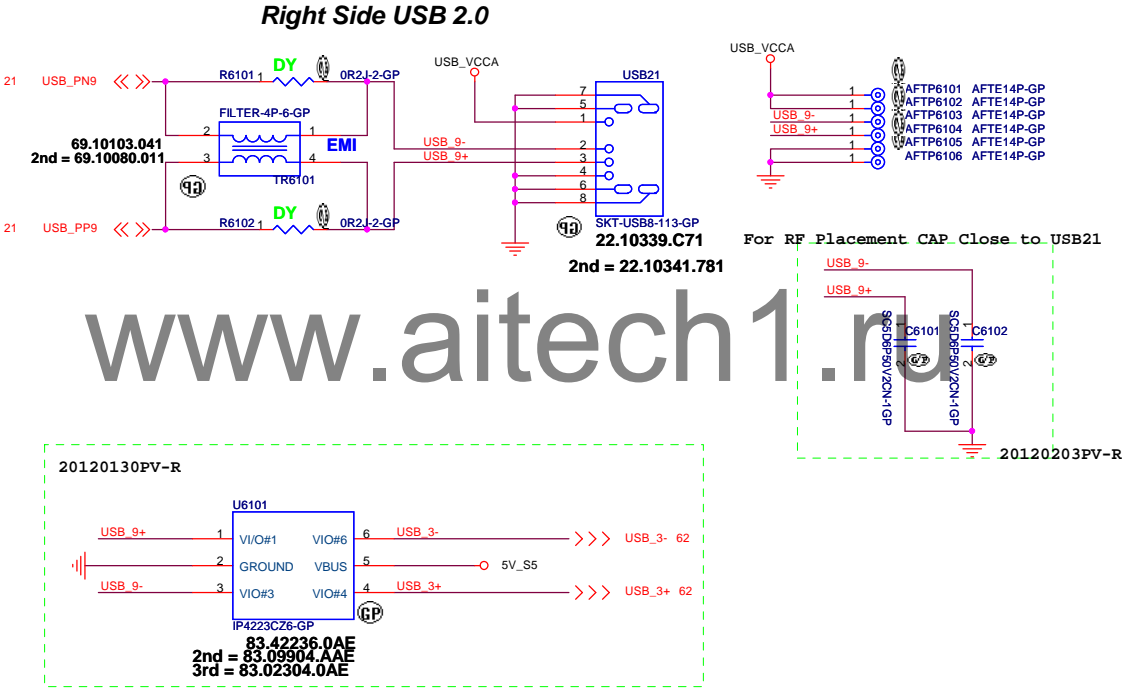
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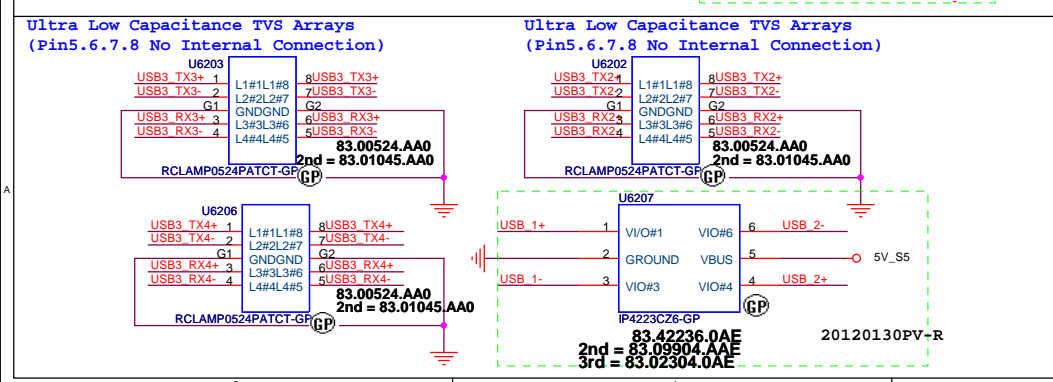
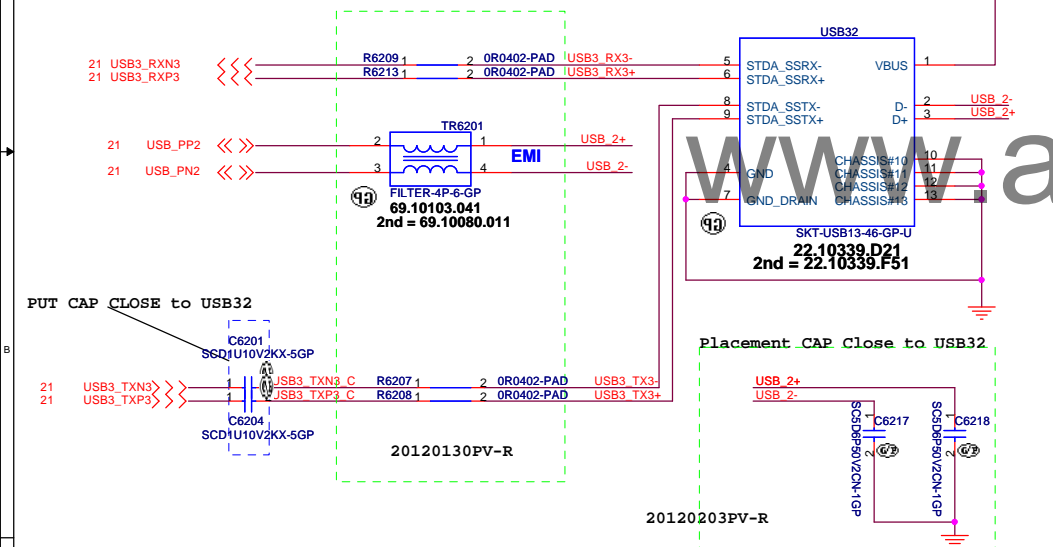
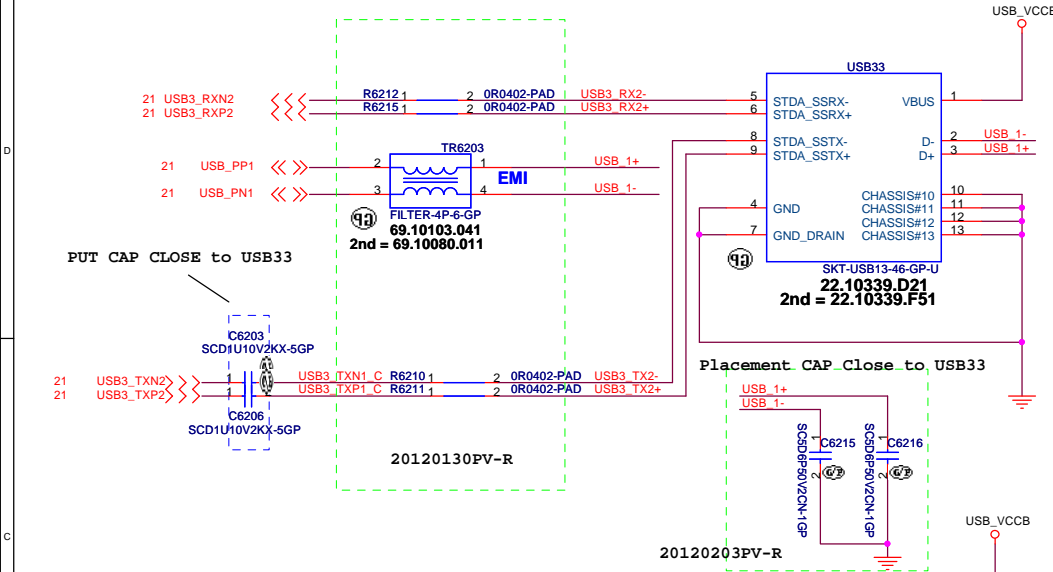
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Right Side USB 2.0 Connector

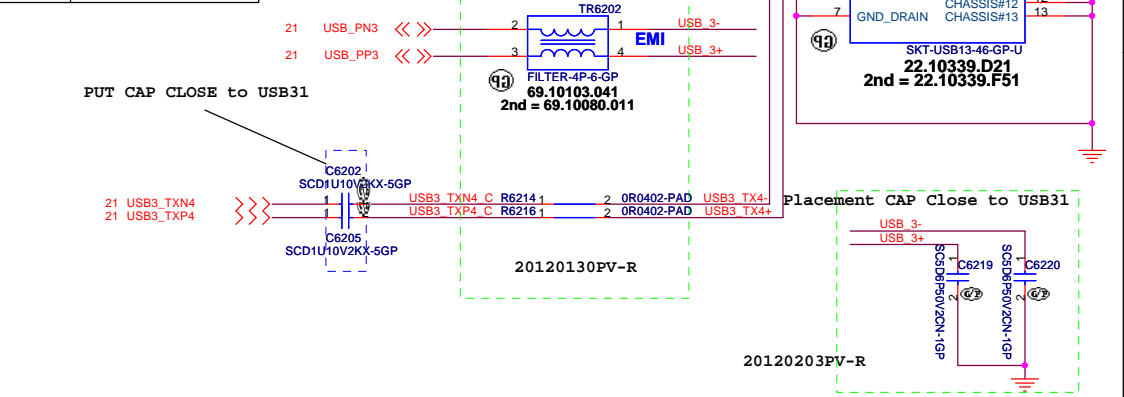


Left Side USB 3.0 Connector

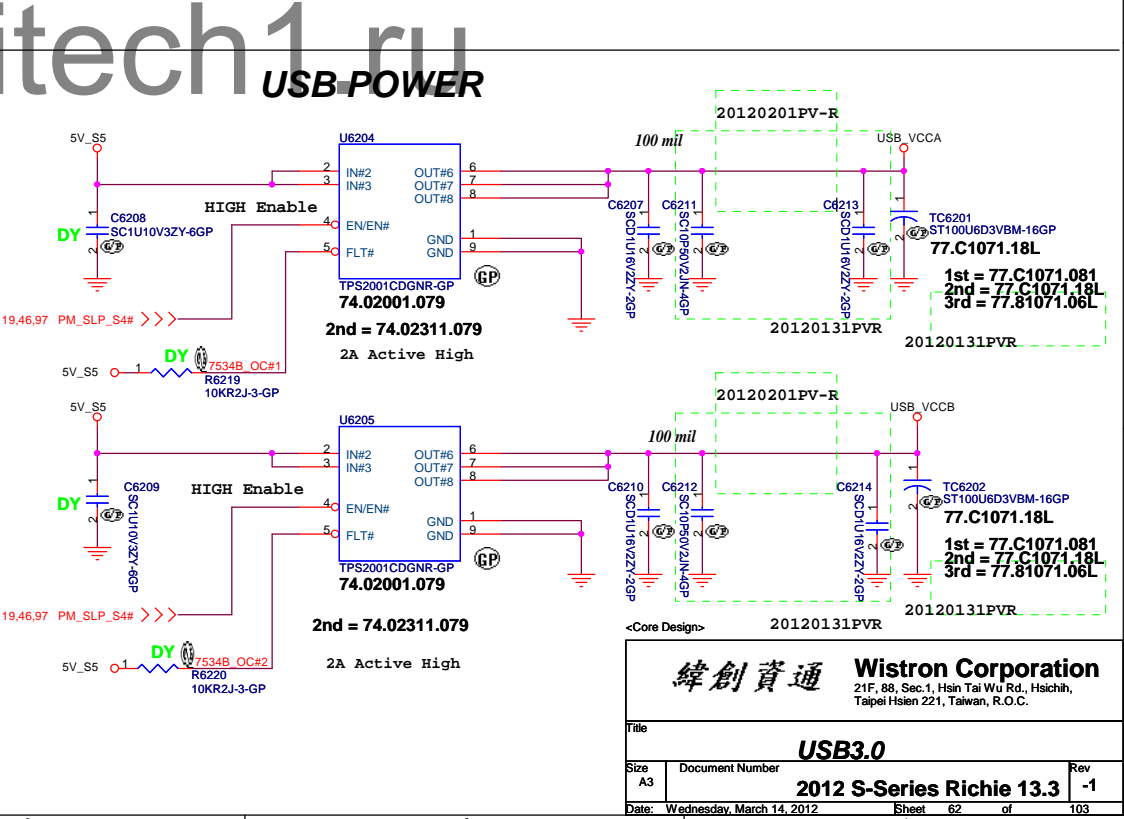


USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+



Right Side USB 3.0 Connector

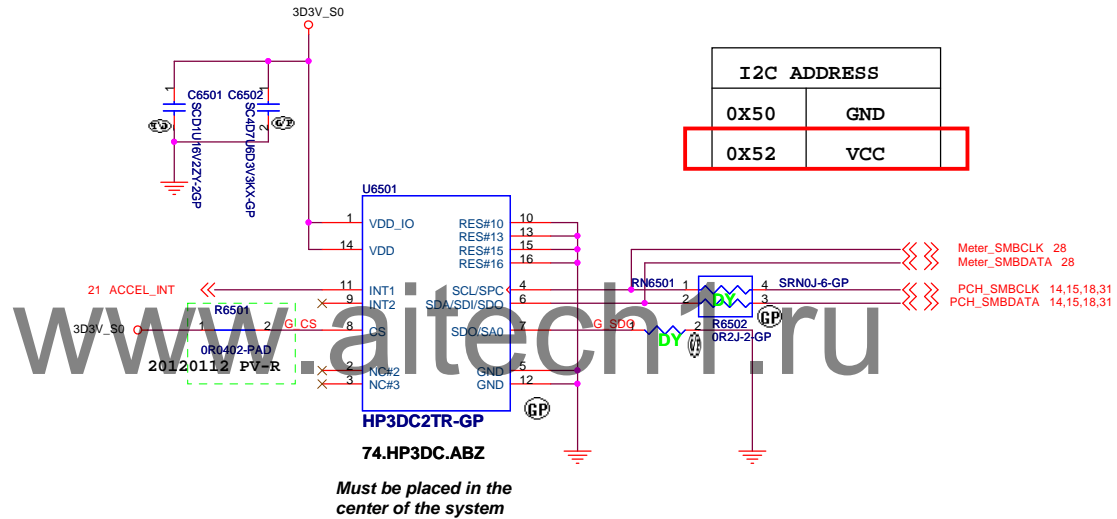


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ACCELEROMETER



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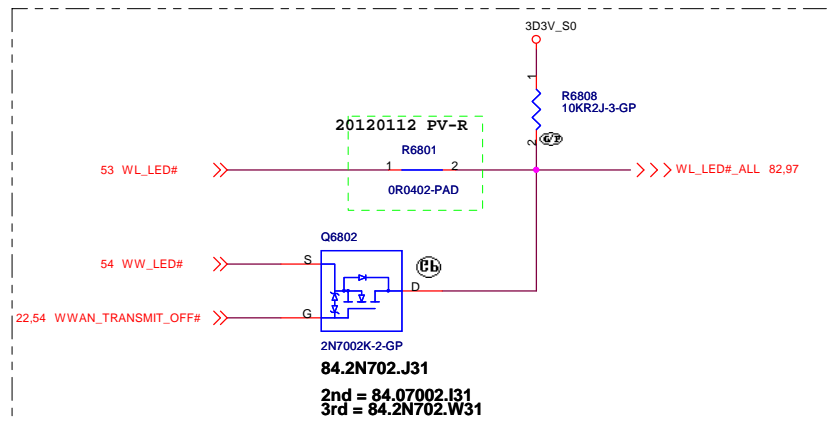
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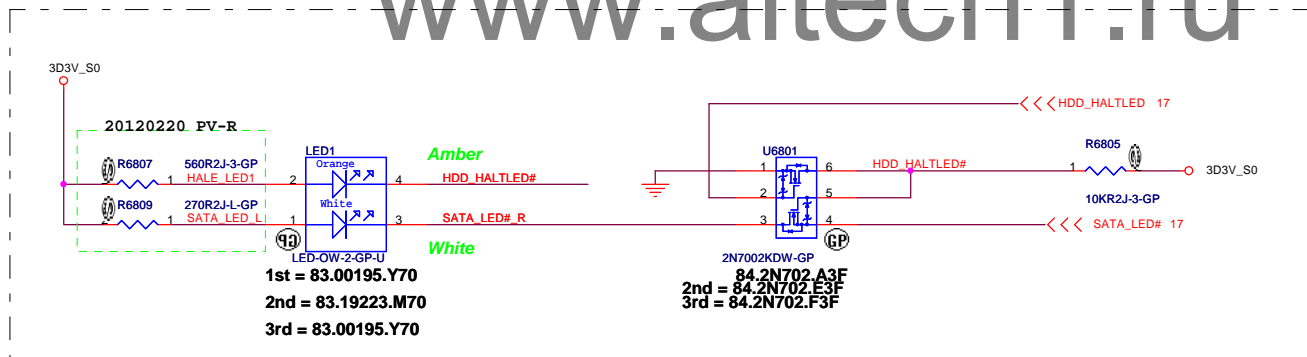
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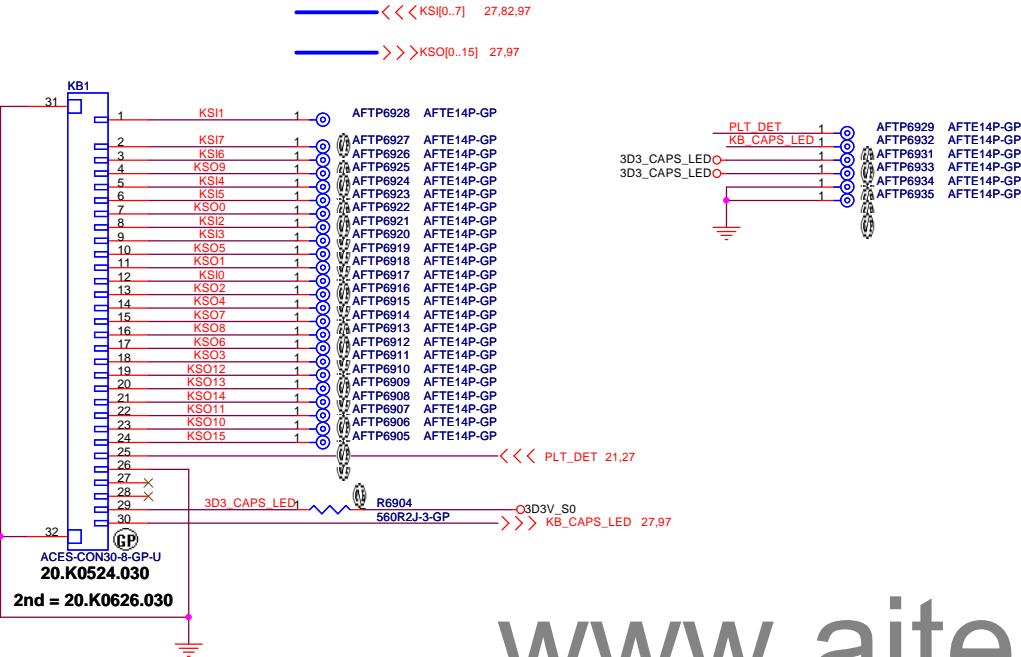


HDD LED



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Keyboard Connector



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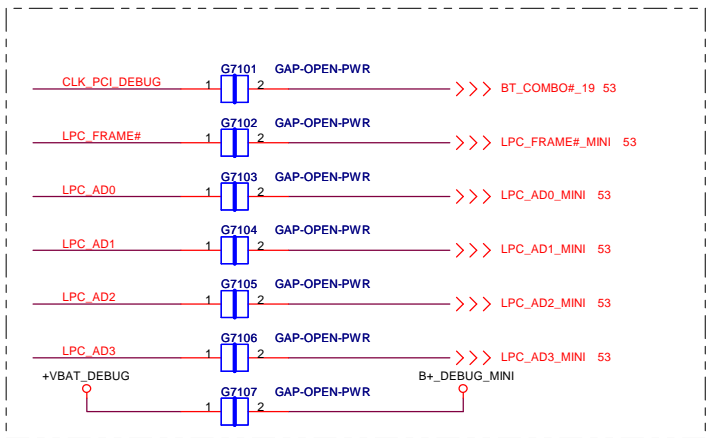
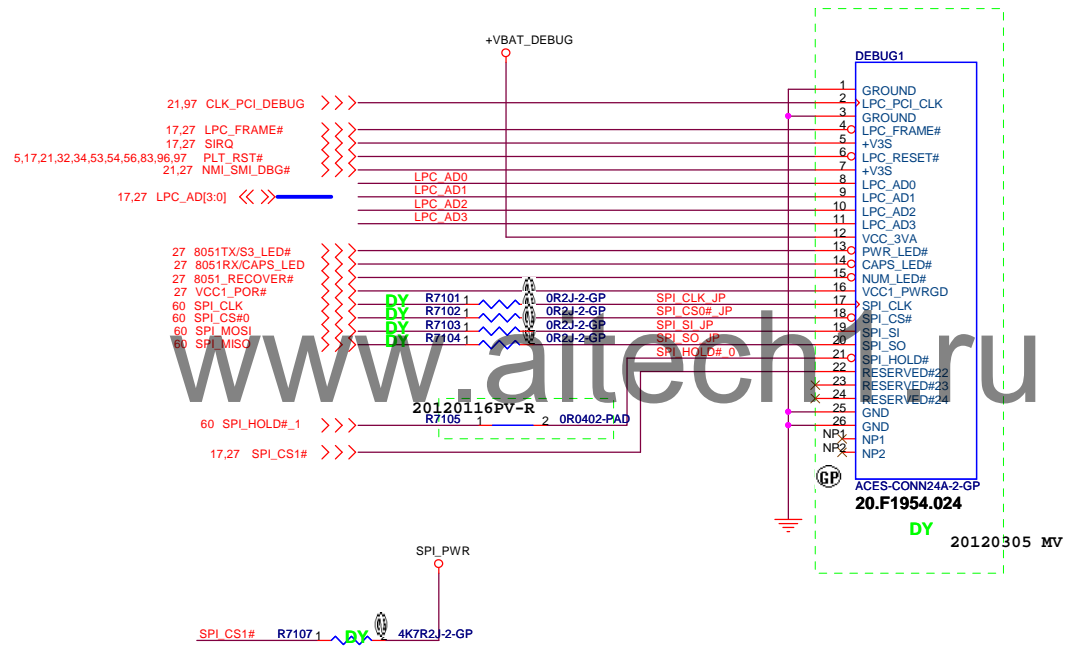
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24 PIN LPC DEBUG CONN.



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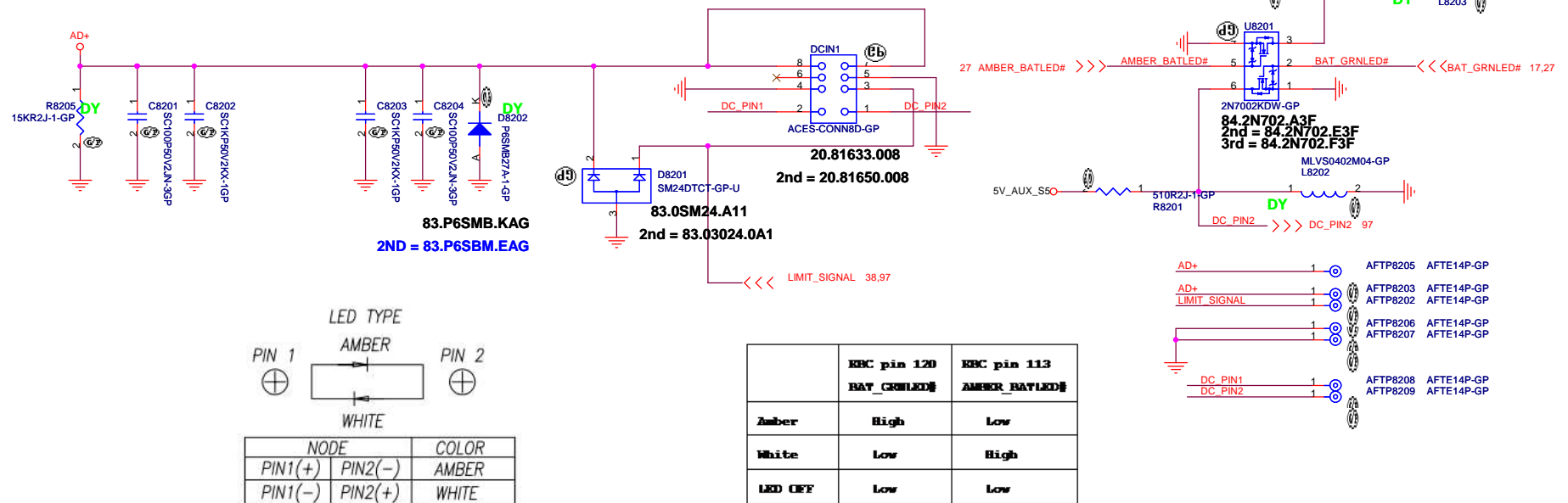
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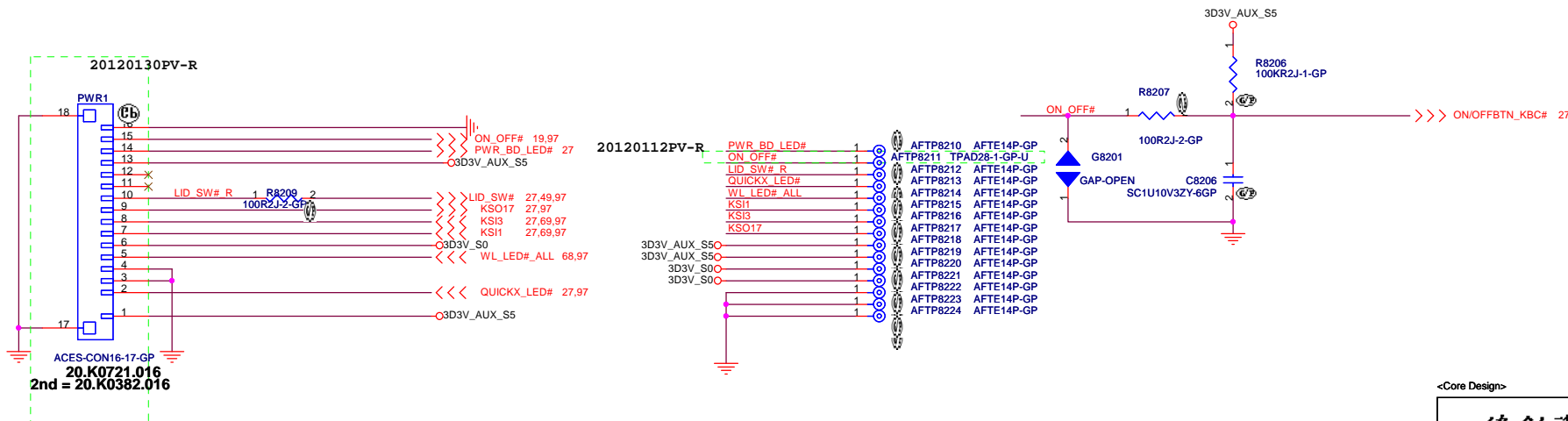
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Adaptor in to generate DCBATOUT



Power Button +Quick Lanch board

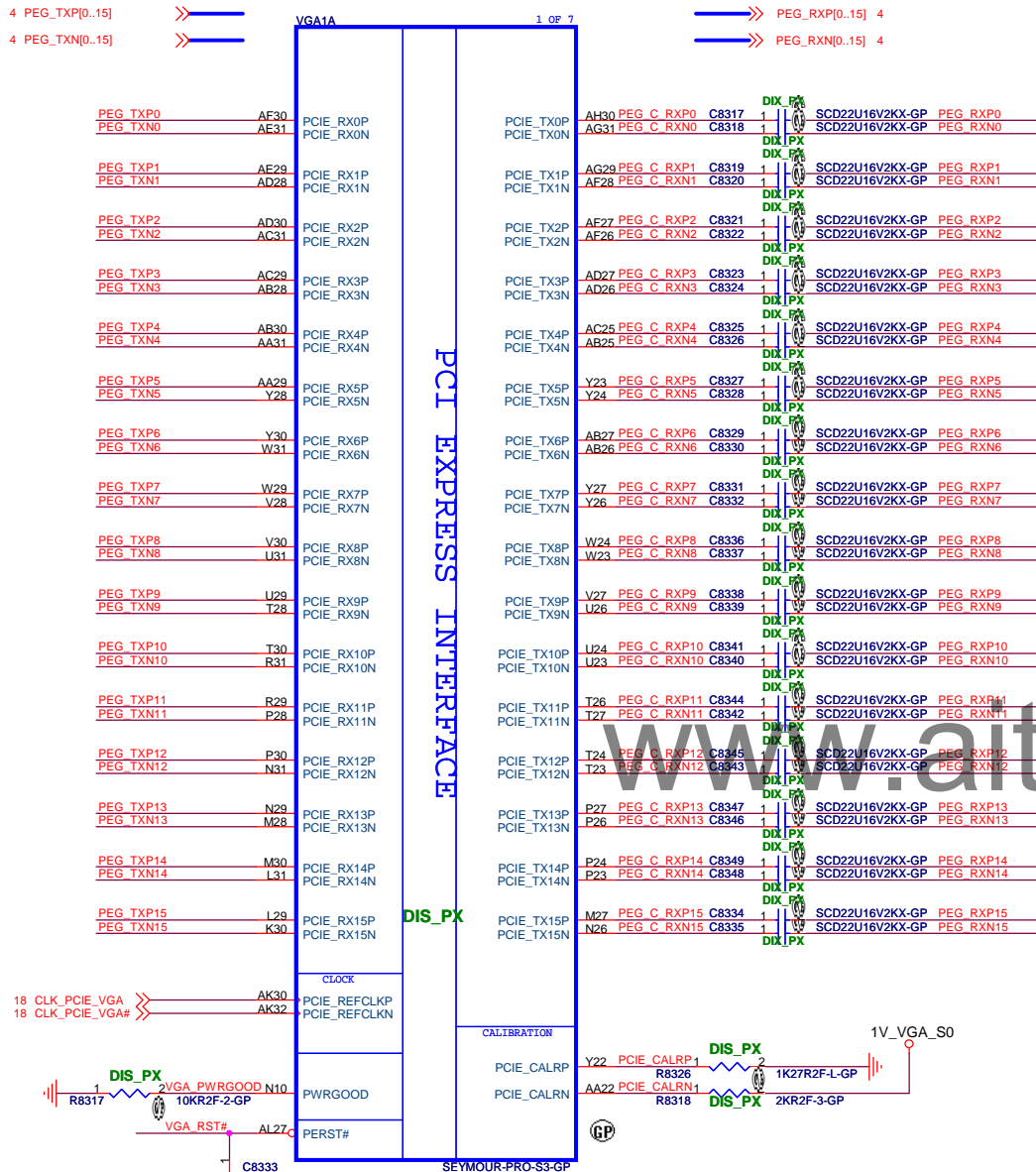
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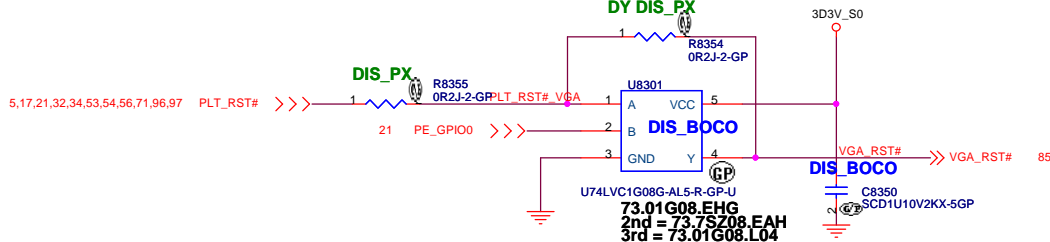
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Title
POWER Button/ DCIN Connector
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dGPU reset for PX/SG transitions

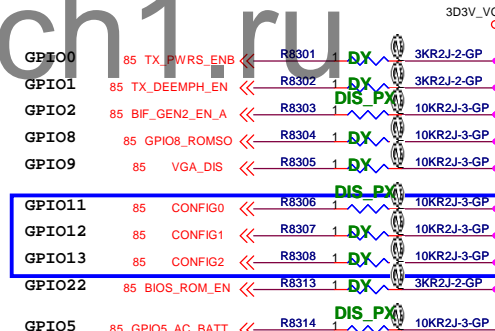


CONFIGURATION STRAPS

ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 3K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSXNC		X	1



GPIO_13	GPIO_12	GPIO_11	Memory Aperture Size
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

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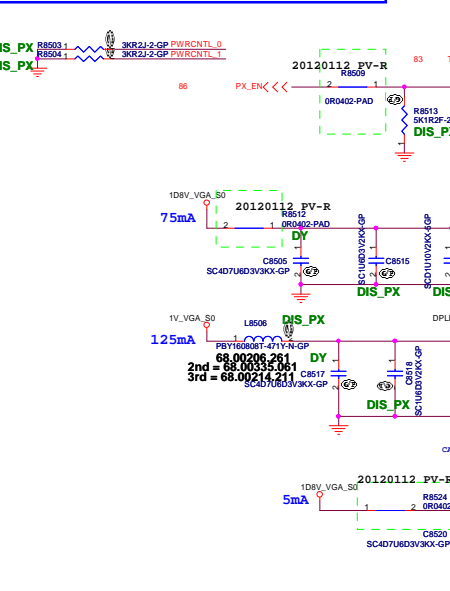
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

MEM ID3	MEM ID2	MEM ID1	MEM ID0	MEM ID VALUE	Vendor & PN	DIE Ver
NC	NC	0	0		Samsung(128X16) K4G2032SFC-HC04	C
NC	NC	1	0	2	Samsung(128X16) K4G2032SFD-FC04	D
NC	NC	0	1	1	Hynix(128MX16) H5SQ2H24A9F-TZC	M
NC	NC	1	1	3	Hynix(128MX16) H5SQ2H24A9F-TZC	A
NC	NC	0	0	0	Elipida(128MX16) E1W2032BBR0-S0-F	B
NC	NC	NC	NC	NC	URA	

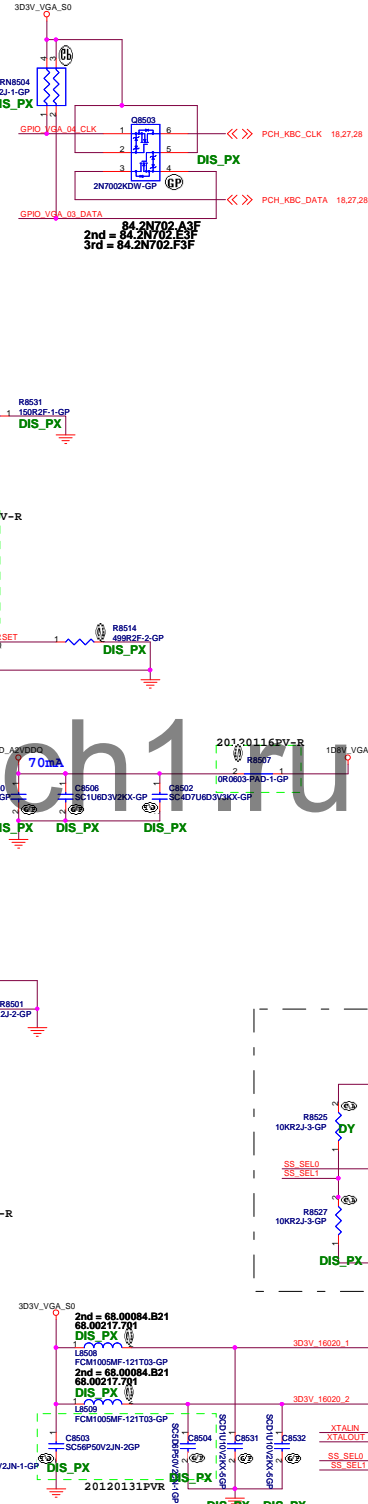
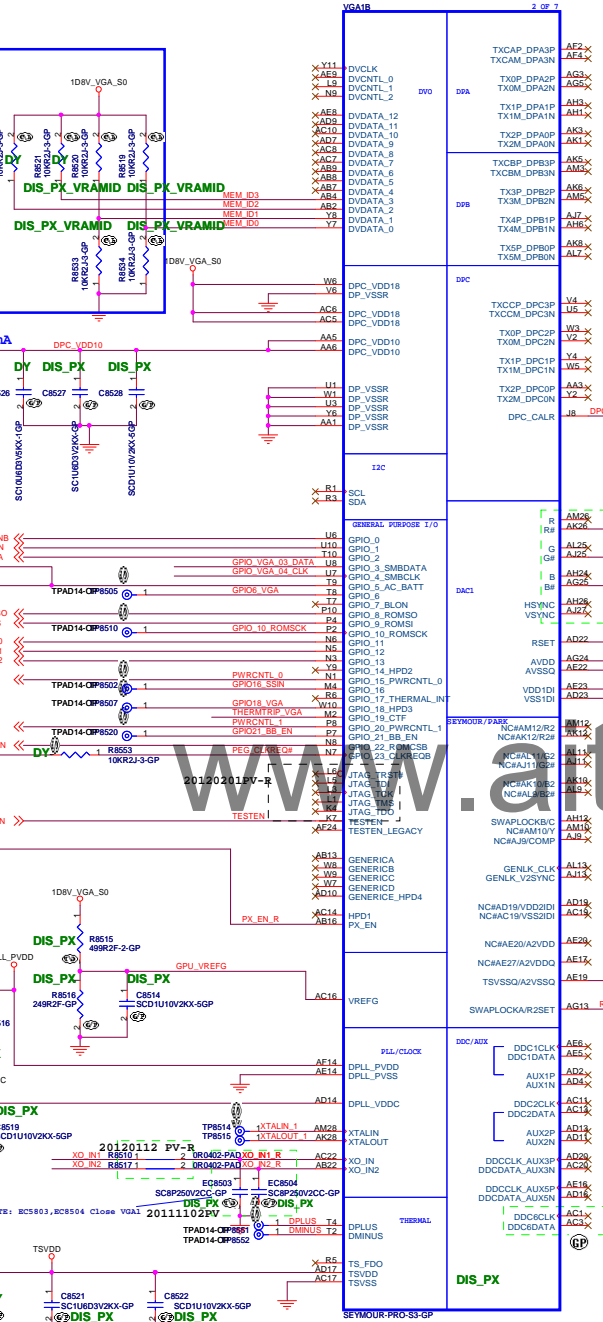
Reserve # = Old Die VRIOS 1 : Samsung
 Pul-High # = New Die VRIOS 2 : Hynix
 Resistor for MEM ID2/MEM ID1 VRIOS 3 : Elipida



GPU SIDE		UP1527Q00D
P10_15_PWCNTL_0	GPIO_20_PWCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V



Memory Type	Description
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and
	100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



VGAIF 6 OF 7

LVIDE CONTROL

VARY_BL
DIGN

AB11
AB12

VARY_BR
DIGN

1 2 3 4

RSN10K15-GP

GP

DM

TXCLK_UP_DPFP3P
TXCLK_UN_DPFP3N

TXOUT_U0P_DPFP2P
TXOUT_U0N_DPFP2N

TXOUT_U1P_DPFP1P
TXOUT_U1N_DPFP1N

TXOUT_U2P_DPFP0P
TXOUT_U2N_DPFP0N

TXOUT_U3P
TXOUT_U3N

LVTXED

DIS_PIX

TXCLK_LP_DPFP3P
TXCLK_LN_DPFP3N

TXOUT_L0P_DPFP2P
TXOUT_L0N_DPFP2N

TXOUT_L1P_DPFP1P
TXOUT_L1N_DPFP1N

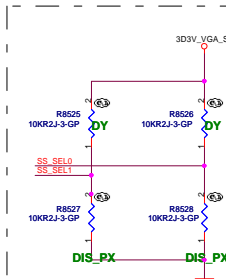
TXOUT_L2P_DPFP0P
TXOUT_L2N_DPFP0N

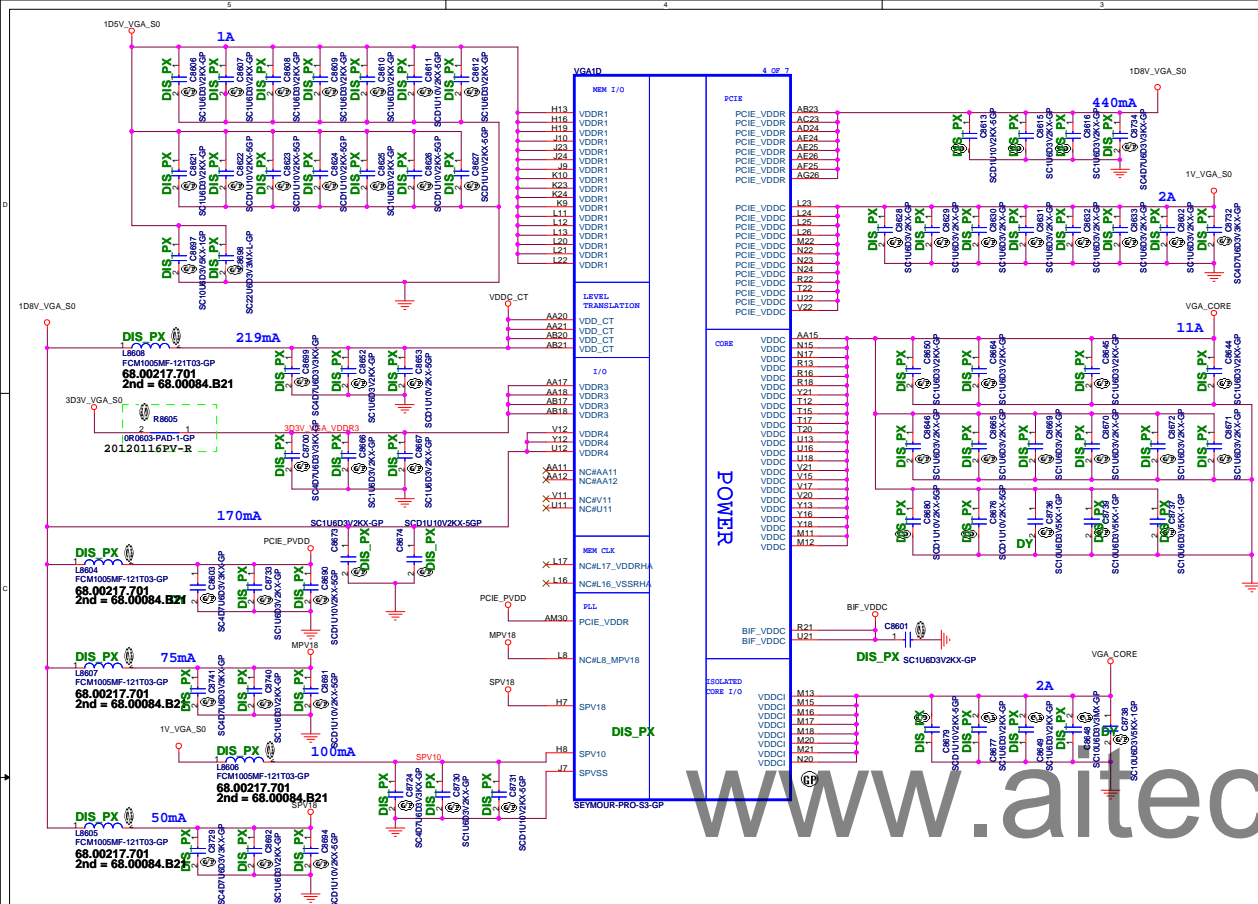
TXOUT_L3P
TXOUT_L3N

GP

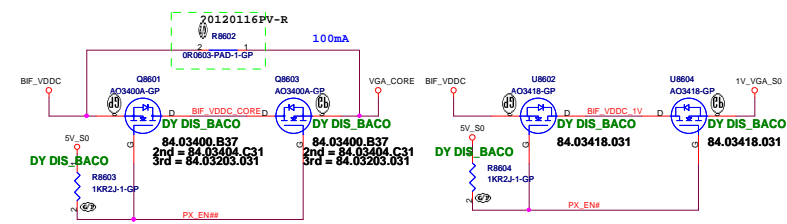
Intel is H_THERMTRIP#

SSEL1 (Pin 3)	SSEL0 (Pin 7)	Spread Percent (%) SSCLK (Pin 5)
Low (VSS)	Low (VSS)	Spread Off (No Spread)
Low (VSS)	Mode (Floating)	-0.50%
Low (VSS)	High (VDD)	-2.9%
Mode (Floating)	Low (VSS)	-0.25%
Mode (Floating)	Mode (Floating)	-0.75%
Mode (Floating)	High (VDD)	-1.0%
High (VDD)	Low (VSS)	-1.5%
High (VDD)	Mode (Floating)	-2.0%
High (VDD)	High (VDD)	-3.0%





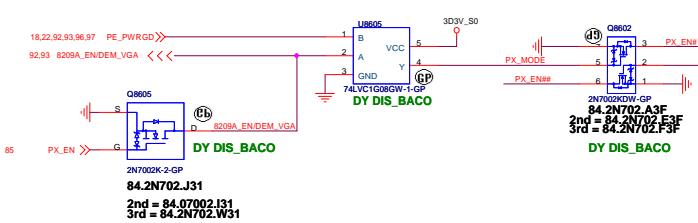
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	PX_EN	B209A_EN/DEM_VGA	PX_MODE	PX_EN#	PX_EN#	BIF_VDDC
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN# = High, BIF_VDDC = VGA_Core

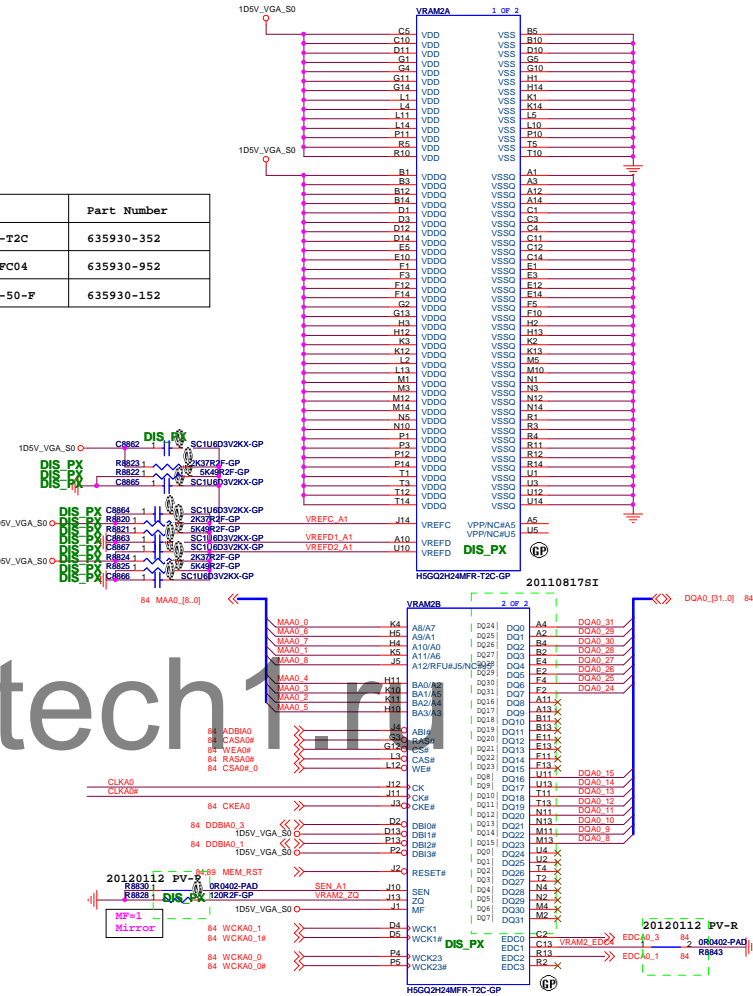
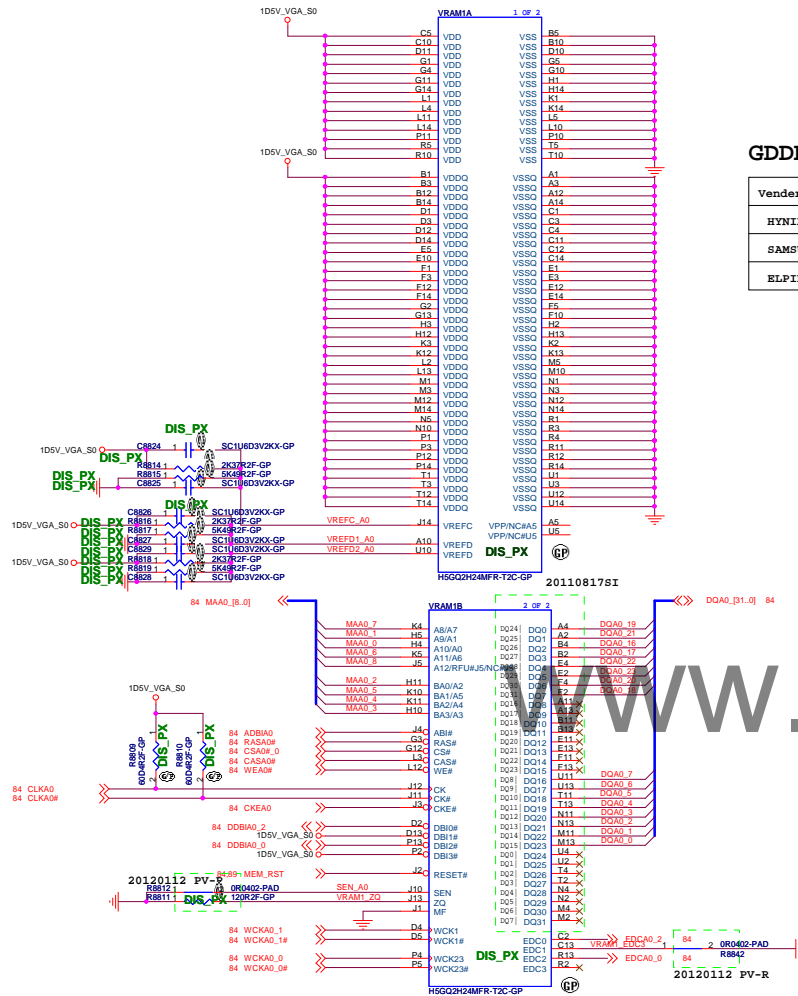
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA



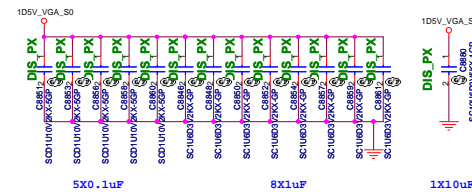
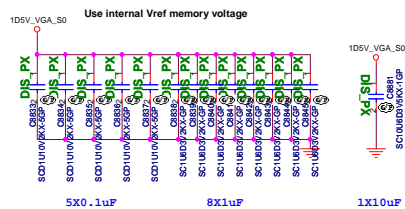


GDDR5 Table

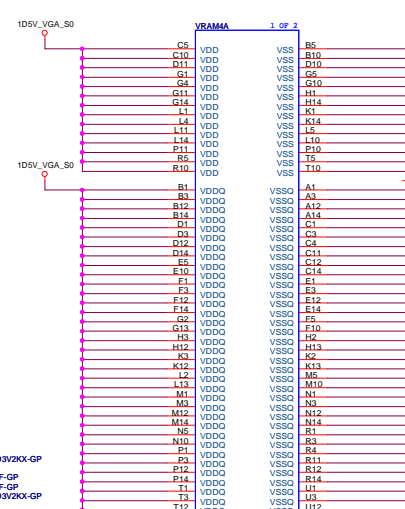
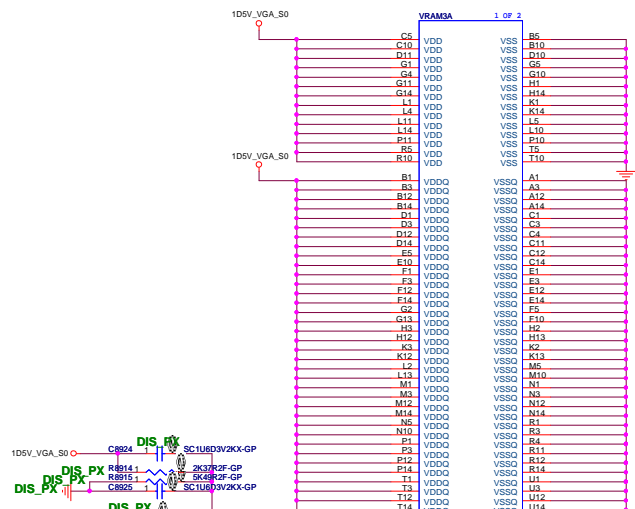
Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24AFR-T2C	635930-352
SAMSUNG	K4G20325FD-FC04	635930-952
ELPIDA	EDW1032BBG-50-F	635930-152



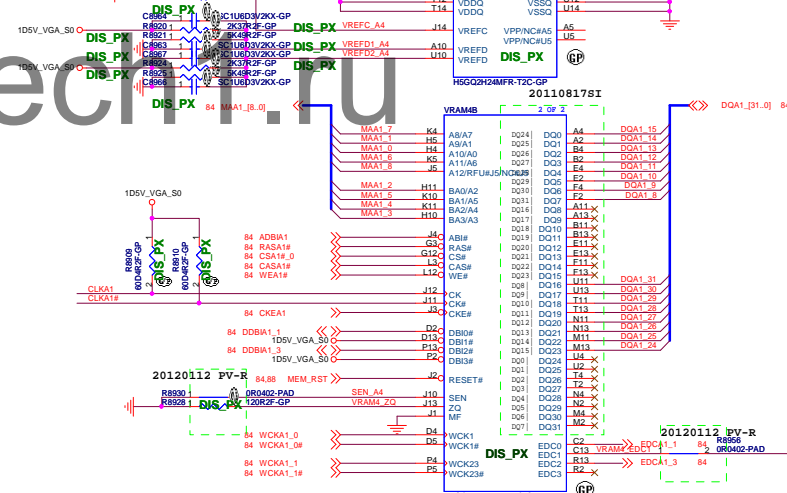
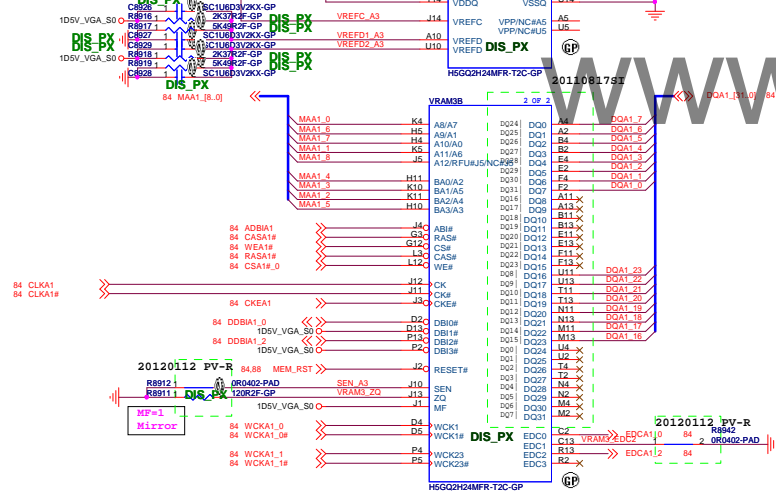
Hynix --> 64M*32



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Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24MFR-T2C	72.05224.00U
SAMSUNG	K4G20325FC-HC04	72.20325.00U



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(Reserved) GPU-VRAM7.8 (4/4)

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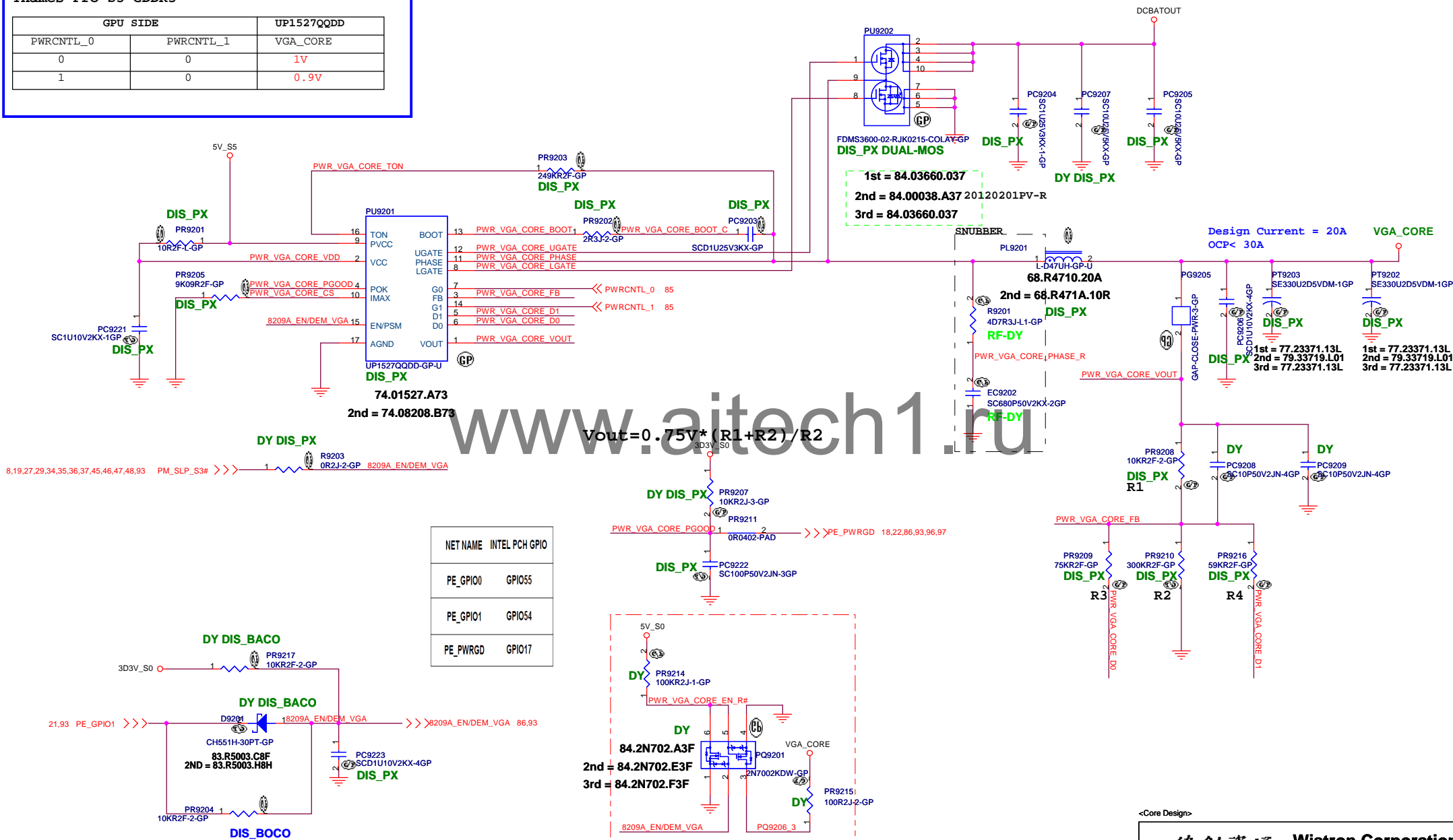
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+VGA CORE

GPU Power ID Table

Thames Pro S3 GDDR5

GPU SIDE		UP1527QDD
PWRCNTL_0	PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V

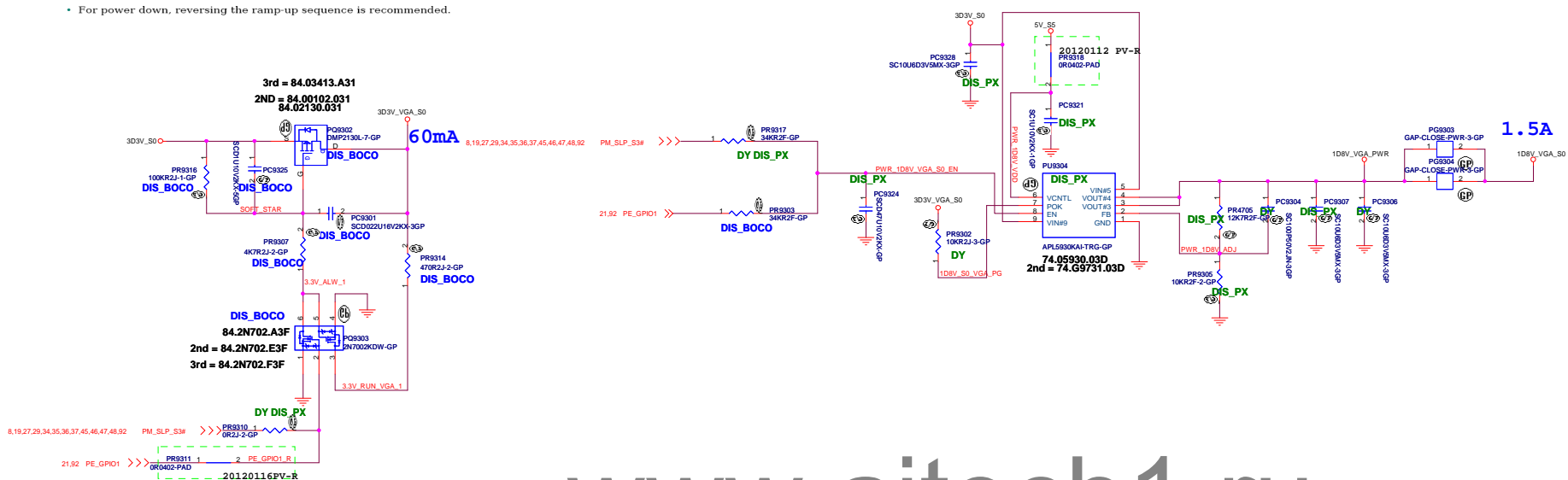


5.3 Power-Up/Down Sequence

Seymour has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

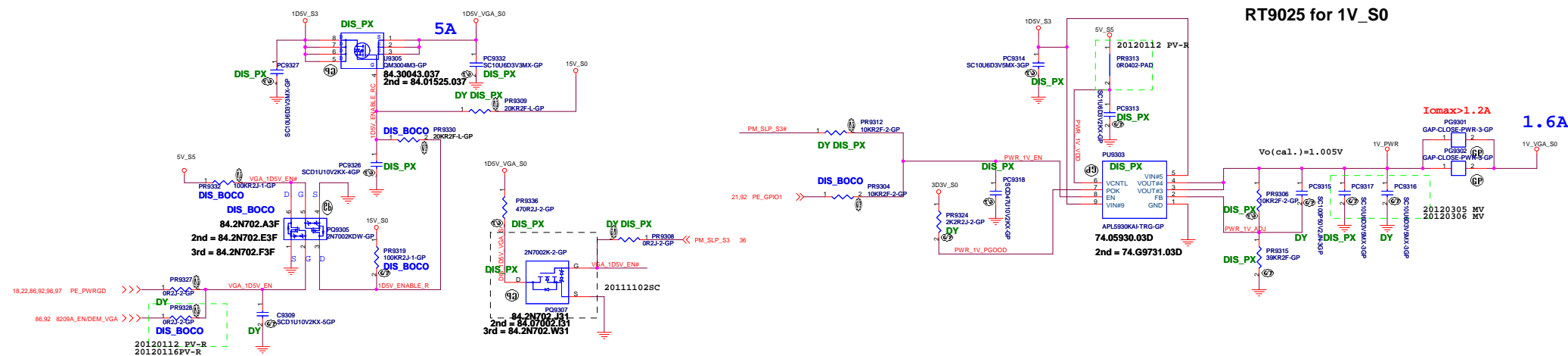
- All the ASIC supply, except for VDDR3, must fully reach their respective nominal voltages within 20 ns of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to the other supply voltages.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDDC and VDDC. CT have ramped up.
- VDDC and VDDC_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDDC_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0




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1D5V VGA S0



<Variant Name>

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DISCRETE VGA POWER			
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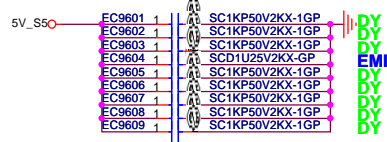
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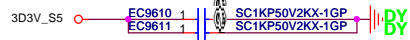
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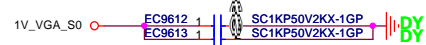
5V_S5 9 PCS



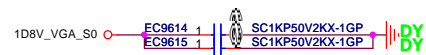
1D8V_PWR 2 PCS



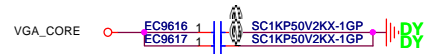
1V_VGA_S0 2 PCS



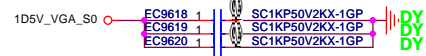
1D8V_VGA_S0 2 PCS



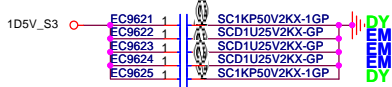
VGA_CORE 2 PCS



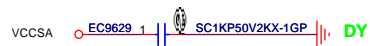
1D5V_VGA_S0 2 PCS



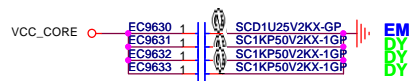
1D5V_S3 8 PCS



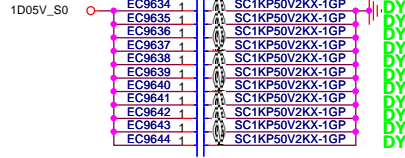
VCCSA 1 PCS



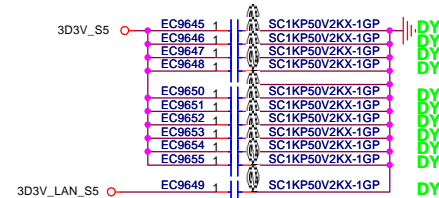
VCC_CORE 4 PCS



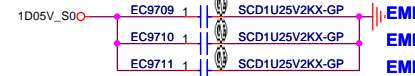
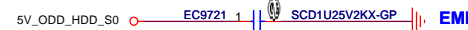
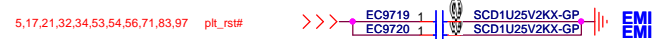
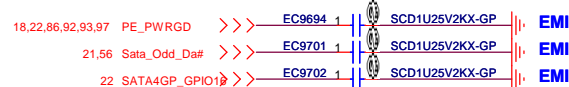
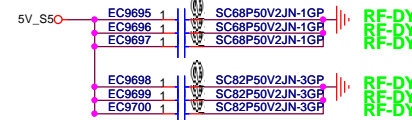
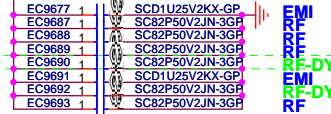
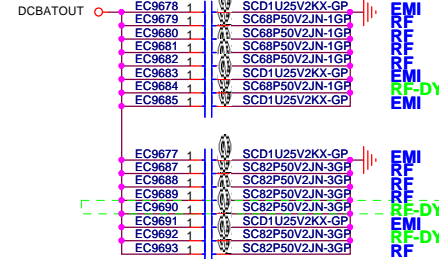
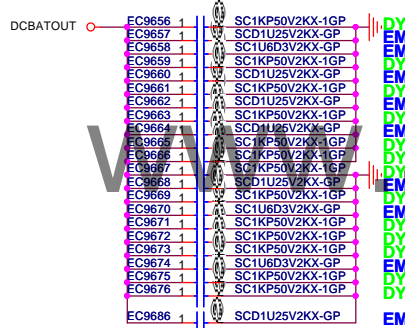
1D05V_S0 11 PCS



3D3V_S5 11 PCS



DCBATOUT 21 PCS



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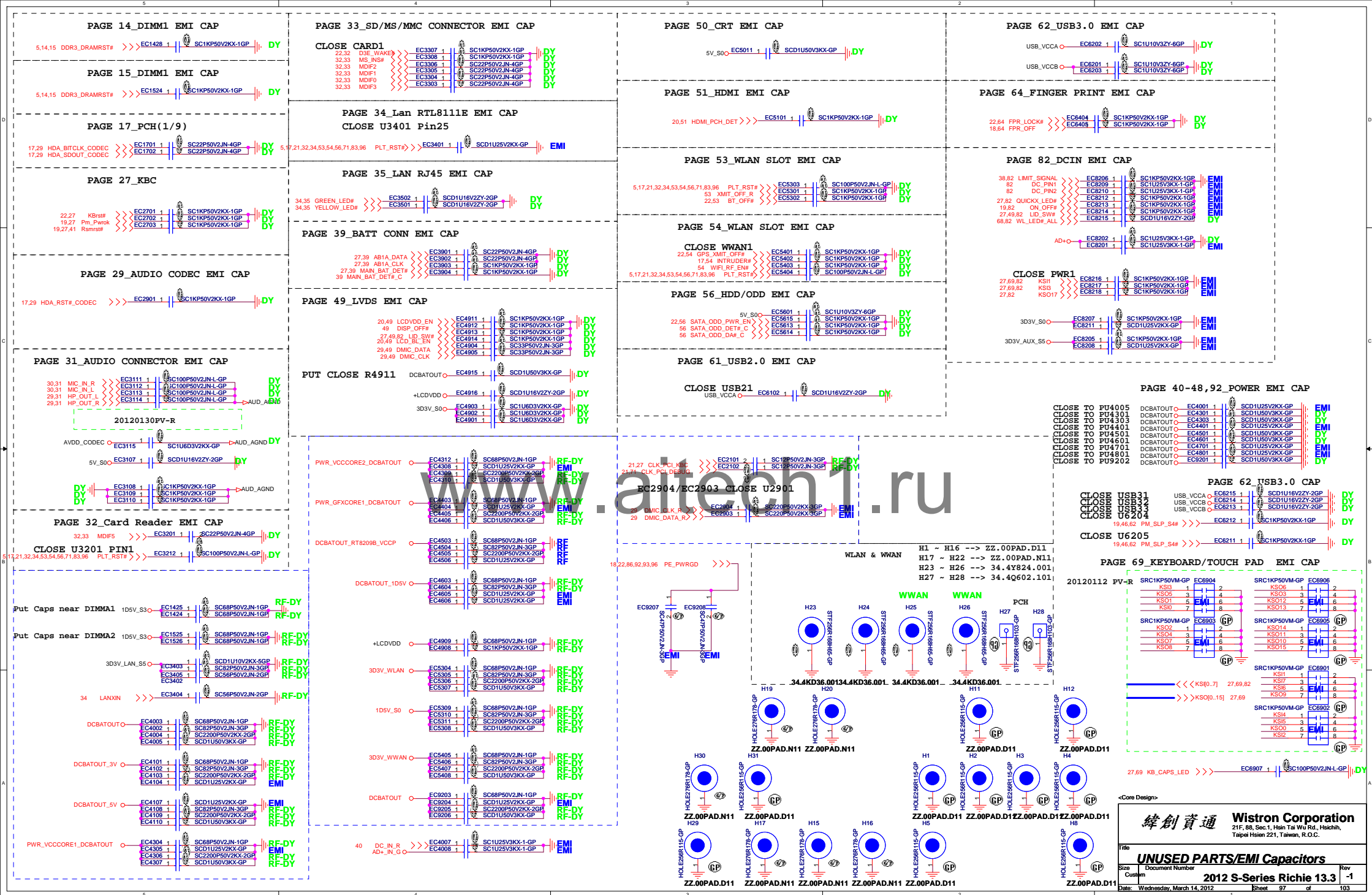
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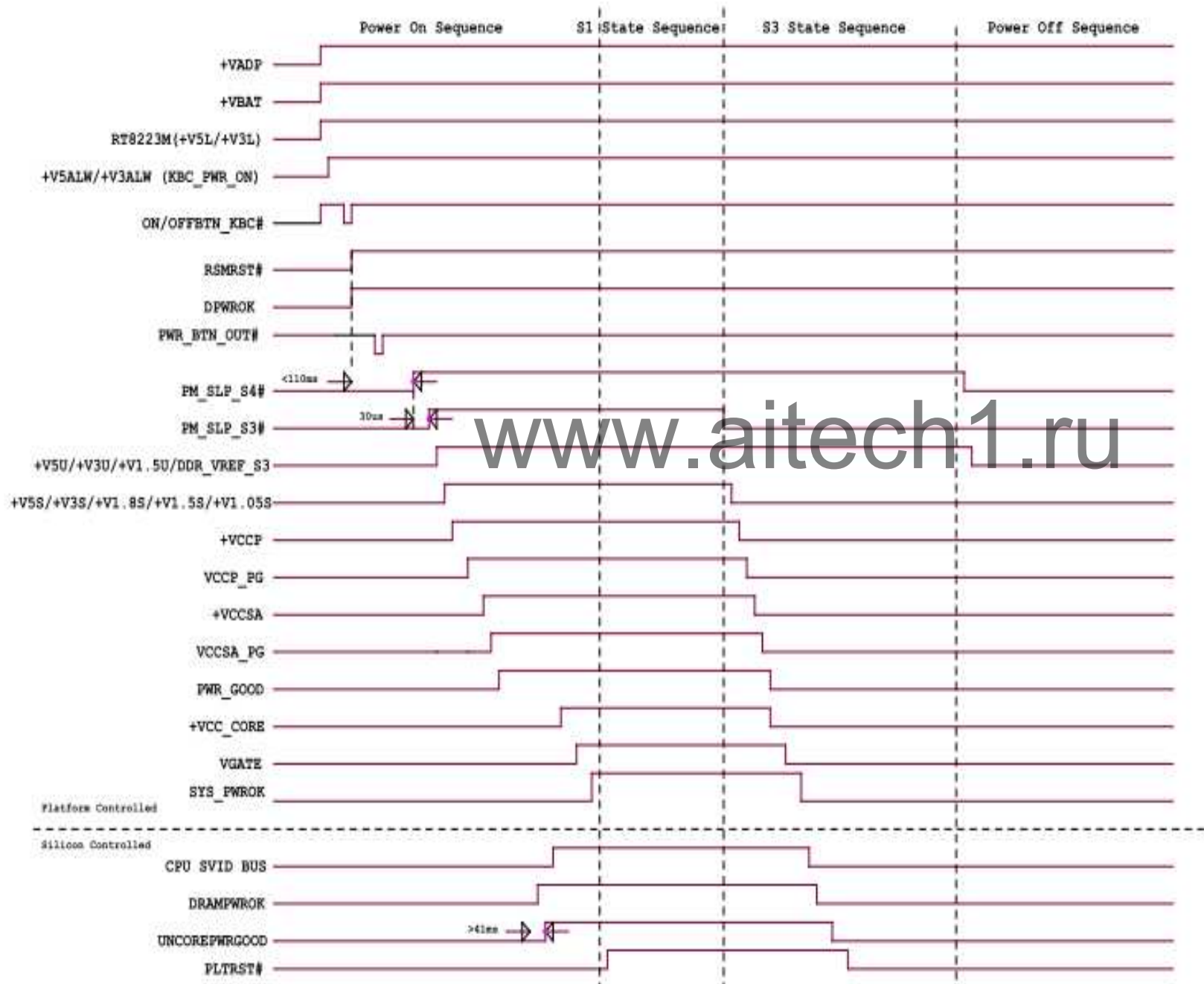
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S-Series Power Sequence and Reset Signal Timing



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Power Sequence

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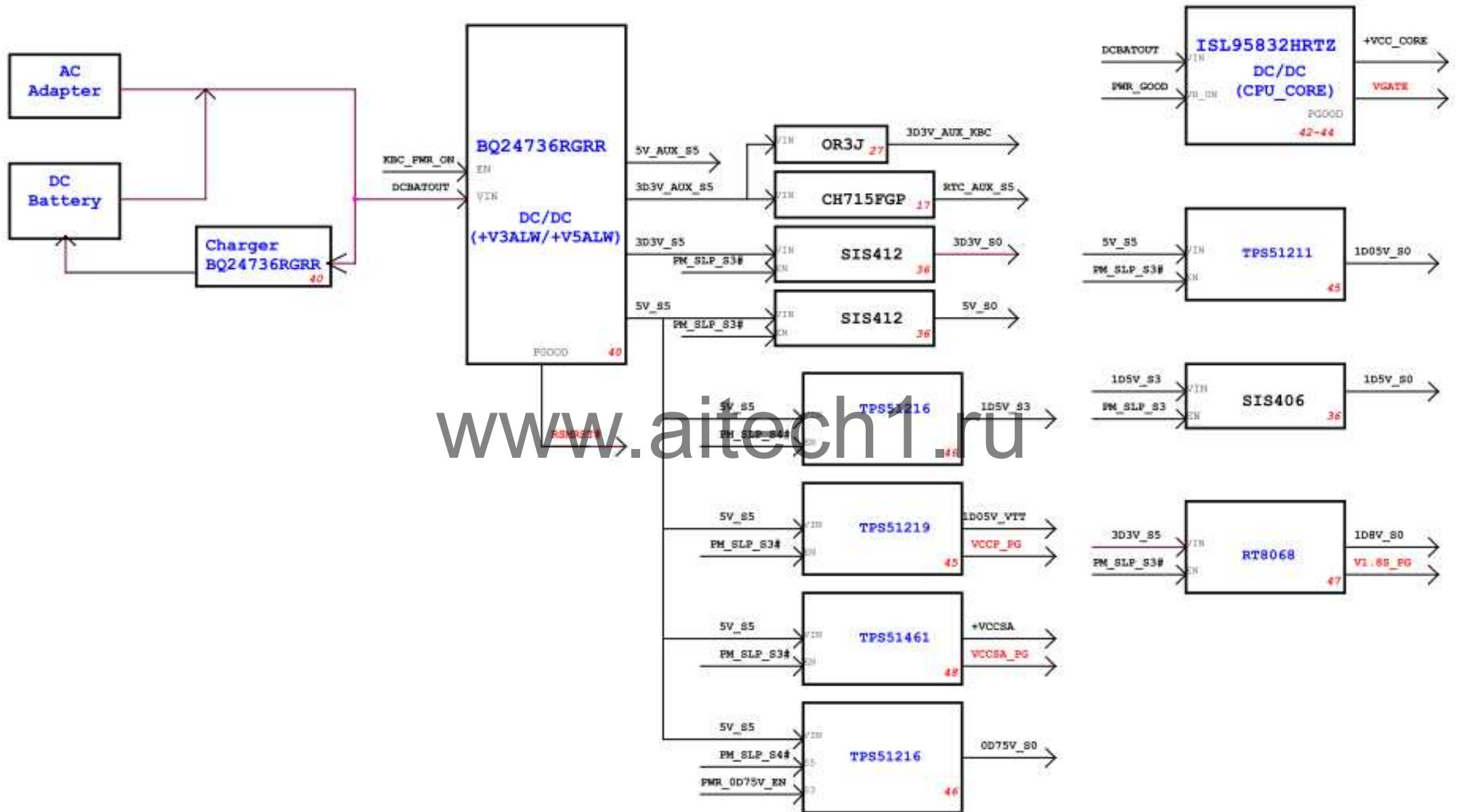
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S-Series POWER BLOCK DIAGRAM

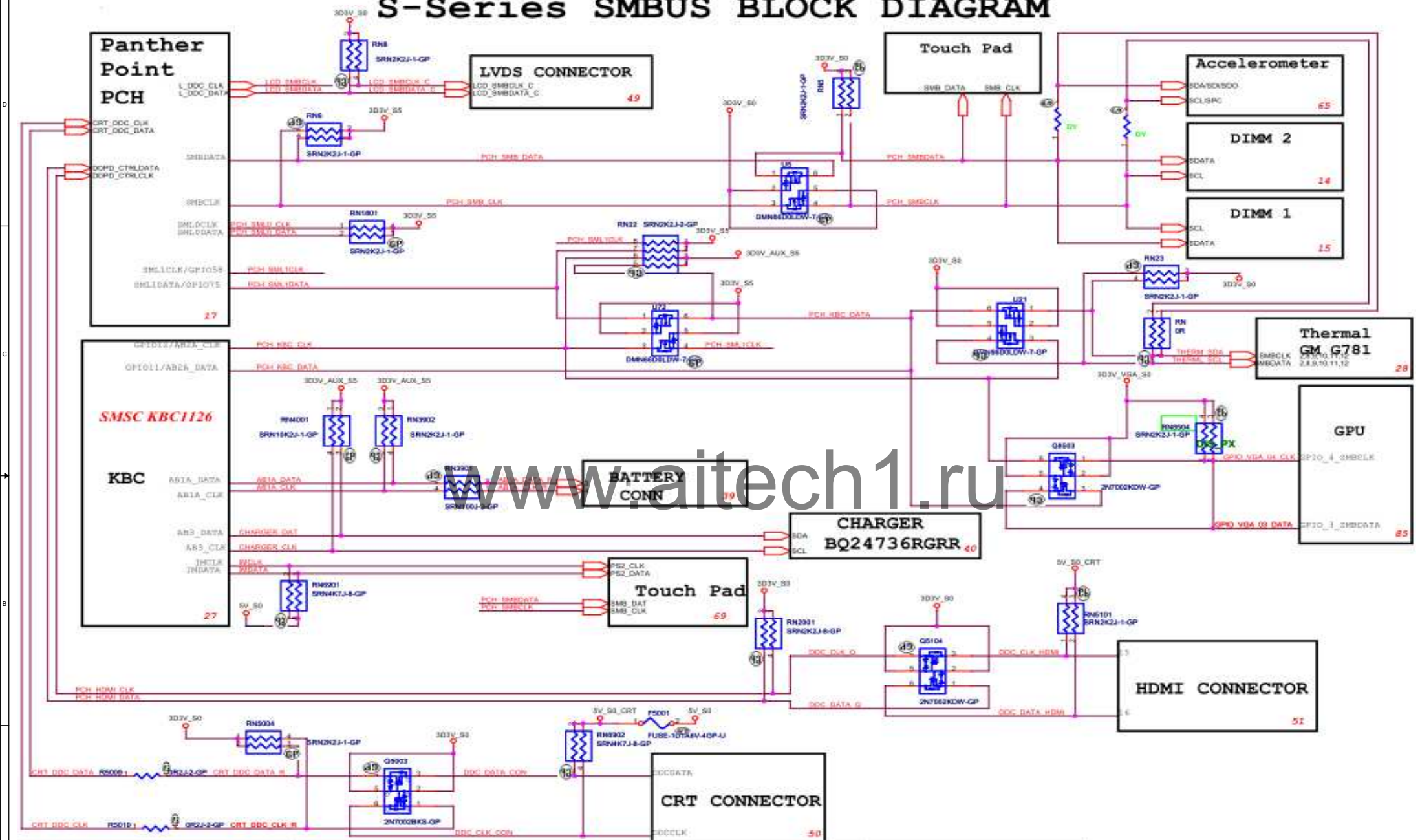


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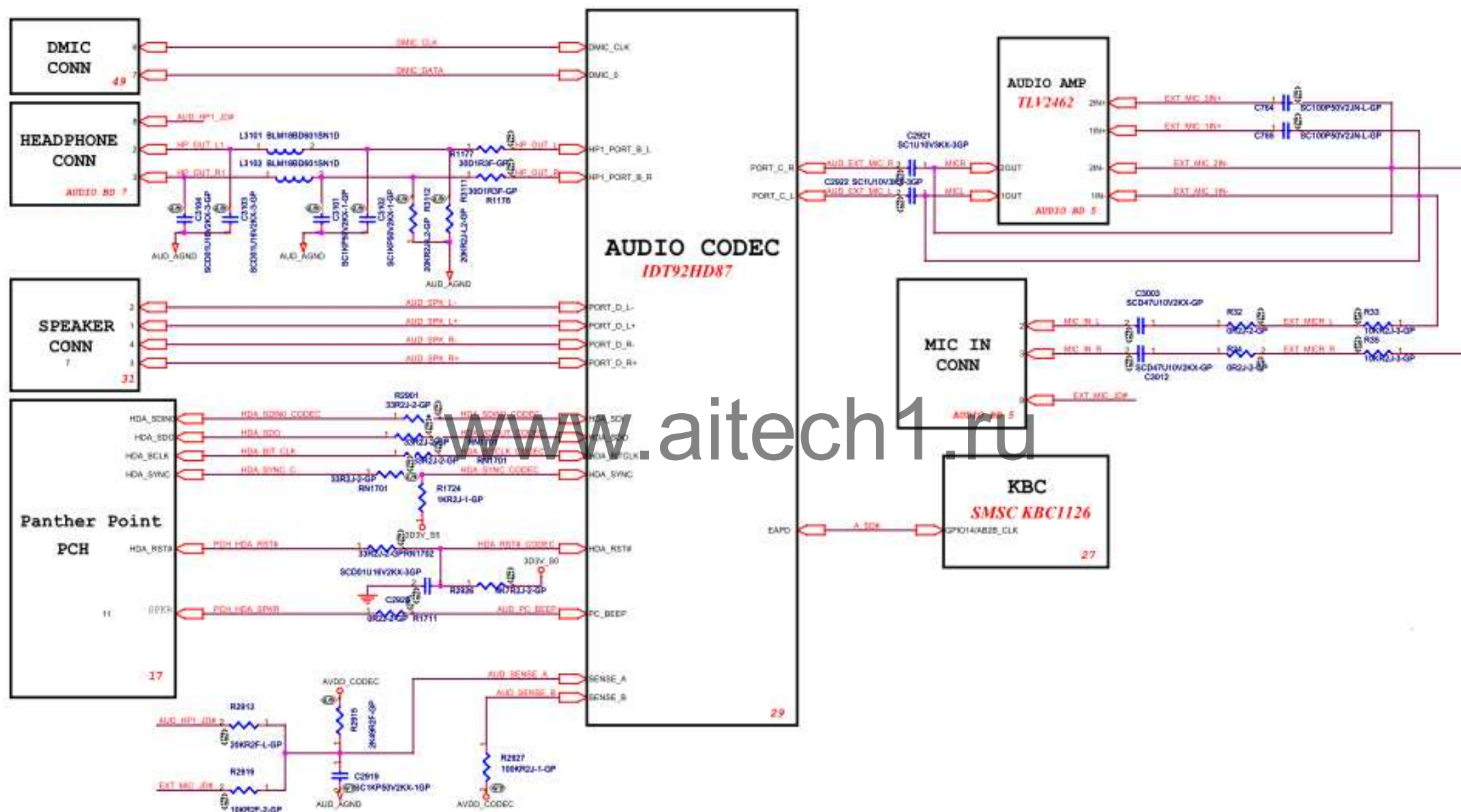
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Power Block Diagram		
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S-Series SMBUS BLOCK DIAGRAM



S-Series AUDIO BLOCK DIAGRAM



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